Institute of Electrical and Electronics Engineers (IEEE)
IEEE Bangalore Section and IEEE Hyderabad Section

IEEE CAS Bangalore Section and IEEE CAS/EDS Hyderabad Section

In collaboration with

Swissnex India

(Connecting Dots between Switzerland and India)

Presents a Technical Session on Mixed Signal Design and Compact Modeling

and

Launch of CFP of IEEE MOS AK India 2019

(IEEE International Conference on Modeling of Systems Circuits and Devices 2019 at IIT Hyderabad)

About the Event:

The technical session consists of two technical talks related to Integrated Circuits and Compact Modeling of Devices. This session is planned as a pre event to promote IEEE International Conference on Modeling of Systems Circuits and Devices (MOS AK India 2019) to be held at Indian Institute of Technology, IIT Hyderabad from 25-27 February 2019. The conference is organised by IEEE CAS/EDS Chapter of Hyderabad Section under the umbrella of MOS AK(www.mos-ak.org) which is a world renowned research group in the area of compact modeling based out of Switzerland that aims at compact modeling R & D Exchange. The Consulate of Switzerland, India (Swissnex, India) and Indian Electronics Semiconductors Association (IESA) are the technical program promoters of this conference. The last version of MOS AK was organised in India in 2012 and it is being brought back after 7 years with the aim of evangelizing model aware VLSI Design. The conference enjoys industry support from ams semiconductors, Global Foundaries, Intel, IBM and other prominent VLSI Design houses.

Technical Talk 1: Current directions in Mixed Signal design

Abstract: In this lecture, we review the current state of the art in Mixed Analog and Digital circuit design. The important building blocks we consider are Filters (switched- capacitor, OTA-C, Continuous-time), A/D converters especially CT sigma-delta converters, Time to Digital Converters, Programmable Mixed Signal arrays for applications like deep learning. New Paradigms such as transistor level designs as against opamp based or OTA based designs with focus on low area and low power consumption will be considered.

Speaker Profile: Dr. P.V. Ananda Mohan received the B.Sc and M.Sc (Tech.) degrees from Andhra University, Waltair, India, in 1965 and 1968, respectively, and the Ph.D degree in electrical communication engineering from Indian Institute of Science, Bangalore, in 1975. He has vast experience in Telecom equipment design especially cartographic systems at I.T.I. Limited and later at Electronics Corporation of India Limited, Bangalore. He has been with CDAC, Bangalore since 2014 as technology Advisor in the area of Information Security and Cryptanalysis. Dr. Mohan is a Fellow of IEEE (U.S.A), IETE (India) and National Academy of Engineering (FNAE). He is currently serving as the Chair of IEEE Circuits and Systems Society of Bangalore Section.

Technical Talk 2: Compact Modeling Technique for Low-Effective-Mass Channel MOSFET

Abstract: Use of low effective mass material (III-V) as MOSFET channel has been in recent focus of the semiconductor industry to deliver higher operating speed under strict power budget. Due to low density of states these devices show strong quantum capacitance effect and thus development of efficient compact models for such transistors is much more challenging than conventional Silicon MOSFET. In this talk we discuss compact modeling techniques that have recently been developed in our laboratory. Based on the Quantum Drift Diffusion (QDD) formalism, we conceive a core model, which combines the solution of coupled Schrodinger-Poisson equation in the transverse direction with classical DD model in the transport direction. QDD has so far been limited to the 'DC-only' device (TCAD) simulation owing to its mathematical complexity. Through our work we pave the way to extend this formalism for circuit (SPICE) simulation. Unlike the existing compact models, here the carriers in each sub-band are treated to be in locally thermal equilibrium within that sub-band, but not with the carriers in a different sub-band. We discuss several innovative methods e.g., analytic solution of coupled Schrodinger-Poisson system, unique charge-linearization techniques, in order to formulate closed-form expressions for drain current and terminal charges. We also demonstrate the implementation of the proposed model in professional circuit simulator.

Speaker Profile: Dr. Santanu Mahapatra received his B.E. (Bachelor of Engineering) degree from Jadavpur University, Kolkata, in the field of Electronics and Telecommunication in 1999, M. Tech (Master of Technology) degree in the field of Electrical Engineering (specializing in Microelectronics) in 2001 from Indian Institute of Technology (IIT) Kanpur, and Ph.D. degree from Swiss Federal Institute of Technology Lausanne (EPFL) in 2005. For his Ph.D. dissertation he worked on the modeling of Single Electron Transistor (SET) and its co-simulation and co-design with CMOS. He joined Department of Electronic Systems Engineering (formerly CEDT), at Indian Institute of Science (IISc), Bangalore, India, as an assistant professor in August 2005 and promoted to associate professor and then full professor rank in September 2010 and December 2015 respectively.

He founded Nano Scale Device Research Laboratory in 2006, where his research team engaged in modeling of carrier transports in nano materials at circuit, device and atomistic level. His research interests include two dimensional channel transistors, energy efficient electronic switches and electrothermal effects at nano-scale. He is the author of the book Hybrid CMOS Single Electron Transistor Device and Circuit Design. He received IBM Faculty award in 2007, Microsoft Research India Outstanding Faculty Award in 2007 and the associateship of Indian Academy of Sciences in 2009. He is also the recipient of Ramanna Fellowship (2012 to 2015) in the discipline of electrical sciences from Department of Science and Technology, Government of India for his contribution in compact modeling. He is a senior member of IEEE (Electron Devices Society) and an editor of the IETE Technical Review journal.

Detailed Program

4.30 PM – 4.40 PM – Welcome Address by Dr. Sebastien Hug, CEO, Consul General, Swissnex India
4.40 PM - 5.20 PM - Technical Talk by Dr. P.V. Ananda Mohan, Fellow IEEE
5.20 PM - 6.00 PM - Technical Talk by Dr. Santanu Mahapatra, IISc Bangalore
6.00 PM - 6.05 PM - Release for Call for Papers of MOS - AK India 2019 by Dr. Sebastien Hug, CEO, Consul General, Swissnex India
6.05 PM - 6.30 PM - Tea and Networking

Date: Friday, 14th September 2018 **Time:** 4.30 P.M to 6.00 P.M
Venue: Seminar Hall, 26 Rest House Crescent Road, Bangalore 560 001, India.
Registration Fee: Nil, but registration is mandatory. Please fill out the google form www.bit.ly/2MvBpEm
Last date for Registration is 7 September 2018. Selected Participants will be intimated by 10th September as we have limited seats.
For any further details please contact:

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