IEEE CIRCUITS AND SYSTEMS SOCIETY BANGALORE CHAPTER

IEEE Bangalore Section

IEEE WiE

Organized by: IEEE CAS Bangalore Chapter
In cooperation with IEEE Bangalore Section and IEEE WiE Council
(IEEE Women in Engineering), Bangalore

IEEE WINTECHCON - 2018

Women's Technical Conference
Women In Technology … 28 September 2018 … 9AM to 5PM
HOTEL ROYAL ORCHID, Old Airport Road, Bangalore

Conference Proceedings

Objective: *To provide opportunities to women technology leaders from India to present their work in emerging knowledge areas*
Theme: Designing the Future Electronic Systems & Applications

Front Matter
Reviewers … Keynote Talks … Tutorials … Invited talk & Panel discussion

Presentations
Session 1.1 : **Vehicular Electronics and Safety** (Paper 12, 73, 77)
Session 2.1 : **System Design - 1** (Paper 18, 44, 27, 34)
Session 1.2 : **Wearbles** (Paper 93, 47, 97)
Session 2.2 : **System Design - 2** (Paper 79, 94, 83)

Posters
Posters -1 (30, 33)
Posters -2 (39, 41, 42)
Posters -3 (43, 48)
Posters -4 (54, 87)

Demo
Demo-1 (2, 82)
Demo-2 (99, 100)

NOTE:
*If this index file **index.pdf** is opened in PDF Reader: Click the PAPER or SLIDES link under each paper to open PDF in a New Tab*
*Click **Allow** if a Security warning gets displayed, and **Yes** in the next to continue*
*If **index.pdf** is opened in the browser: Click links to open in the same Browser window*
*Or **Ctrl-click** the Paper or Slides links to open in a New tab/Window without closing the index*
*Or locate the concerned file under the **papers** folder to click-open*
(the required file can be identified under the categorized subfolders)

HOME

COMMITTEE

Steering Committee:

- Roopashree H.M., Texas Instruments (Chair)
- C.P. Ravikumar, Texas Instruments (Advisor)
- Viji Ranganna, Qualcomm
- Rituparna Mandal, MediaTek
- Sumedha Limaye, Intel
- Jaya Singh, Texas Instruments
- Parvathi Rachakonda, IBM

Technical Committee:

- Rittu Sachdev, Texas Instruments
- Neha Vernekar, Texas Instruments
- Juby Jose, Intel
- Ranjini M, Texas Instruments
- Anjana Ghosh, Canon
- Dr. Seema Chopra, Boeing
- Chaitra M Bhat, IBM
- Divya K Konoor, IBM
- Mousumi Baruah, Bosch
- Sunitha Cherkottu, Texas Instruments
- Mithula Madiraju, IBM
- Garima Srivastava, Samsung
- Krishna Paul, Intel
- Jiji Jayadevan, Mediatek
- Raka Singh, Analog Devices
- Deepti Varadarajan, MediaTek

Organizing Committee:

- Mitu Misha, Texas Instruments
- Suhasini Singh, Texas Instruments
- Antaash Sheikh, Texas Instruments
- Annapurna Patil, IEEE WiE, Bangalore
- Deepa Shenoy, IEEE WiE Bangalore
- Sidhartha Mohanty, Intel

INTENT

Diversity is a much discussed issue in engineering. The good news is that based on a recent directive of the Ministry of HRD, more than 30 premier educational institutions including IITs and NITs will admit more women in their programs. In fact, these institutions have been directed to admit at least 14% women students.

Today, every technology giant has a diversity program to track and influence hiring, and promote the growth of women in technology. In many countries, the number of women opting for engineering education has dwindled over the years. Fortunately, India is not one of them. Prior to the 1980s, engineering curricula across the country were dominated by Civil and Mechanical Engineering and High-Voltage Electrical Engineering. The number of girl students attracted to these branches of engineering was small. With the introduction of a large number of programs in electronics and communication engineering, computer science and Information Technology in the 1990s, the situation changed dramatically. In addition to a growing number of student enrollments, we also see a growth in women faculty in engineering colleges. There are also several engineering colleges in India exclusively for women.

There are several established technology conferences in India today. Many of these are organized by IEEE. To provide an exclusive forum for women in the technology space to present their work, demonstrate their DIY projects and network with engineers from other organizations, IEEE CAS Bangalore haD organized WINTECHCON-2018 in association with IEEE WiE and IEEE Bangalore Section.

This was the first such event to be held in the city. We hope the event will grow in the future. The objective of the conference is to provide opportunities to women technology leaders from India to present their work in emerging knowledge areas.

REVIEWERS

HOME

Abhishek Ghosh, Samsung
Abir Chakraborty, AI
Anand Bodas, Intel
Anbumani Subramanian, Intel
Anjana Ghosh, Canon
Arpan Sircar, Intel
Ashok Balivada, Analog
Ashwini Khandekar, Intel
Atanu Talukdar
Atul Lele, Texas Instruments
Bharathi V, Intel
Bijesh Poyil, Analog
C.P. Ravikumar, Texas Instruments
Chaitra M Bhat, IBM
Chhavi Agarwal, IBM
Debapriya Sahu, Texas Instruments
Debasish Deb, LRDE
Deepti Varadarajan, MediaTek
Divya K Konoor, IBM
Dr Rafal Baranowski, Bosch
Dr. Seema Chopra, Boeing
Garima Srivastava, Samsung
Guha Lakshmanan, Canon
Halasya Siva Subramania, Boeing
Harikrishna Parthasarathy, Texas Instruments
Harinarayanan Seshadri, Intel
Indu Prathapan, Texas Instruments
Jaiganesh Balakrishnan, Texas Instruments
Jaya Singh, Texas Instruments
Jayashri AB
Jeyanthi Jegadeesan, Analog
Jiji Jayadevan, MediaTek
Juby Jose, Intel
Kalpana P, PSG Tech
Kalyan Chakravarthi Chekuri, Texas Instruments
Kannan Babu Ramia, Intel
Kapil Agrawal, Intel
Karthik Subburaj, Texas Instruments
Kirti Keshav, Samsung
Krishna Paul, Intel
Krishnaswamy T, QTI
Madhusudanan Kandasamy, IBM
Mahalakshmi SB, GE
Manoj Ariyamparambath
Mithula Madiraju, IBM
Mohit Tahiliani, NITK
Mousumi Baruah, Bosch
Narayan Ranganathan, Intel
Neeraj Bhardwaj, Texas Instruments
Neha Vernekar, Texas Instruments
Neil Deshpande, Samsung
Niloy Ganguly
Ophir Shabtay, Intel
Parvathi Rachakonda, IBM
Poornima Sathyanarayana, IBM
Prakash Narayanan
Rajashree Srinidhi, Rambus
Raka Singh, Analog Devices
Rakesh Hariharan, Texas Instruments
Rakesh Kumar, Steradian Semiconductors
Rama Kowsalya Namburi, Canon
Raman K, analog
Ranjini Mukunda, Texas Instruments
Rathish Balagangadhar, Samsung
Ritesh Rajore
Rittu Sachdev, Texas Instruments
Rituparna Mandal, MediaTek
Roopashree H.M., Texas Instruments
Rugmini K, Analog
Rupak Ghayal, Maxlinear
Saahithyan Radhakrishnan, Samsung
Sailesh Rathi, Intel
Sankaran Aniruddhan, IITM
Satish Muthiyalu, Intel
Saurabh S, Analog
Saurabh Tiwari, Intel
Seema Chopra, Boeing
Sheena K P, Canon
Shekhar Sharma, Samsung
Shivashankar Gangadhar, GE
Shyam Kalakat, Broadcom
Somu Ghosh, Texas Instruments
Soumen Sarkar, Intel
Sridhar Rangarajan, Mentor
Sriram Ganapathi, IISc
Subrangshu Das, Intel
Sumedha Limaye, Intel
Sundarrajan Rangachari
Sunitha Cherkottu, Texas Instruments
Suresh Papneja, Ericsson
T Krishnaswamy, QTI
Trupti Joshi, Intel
Veeramanikandan Raju, Texas Instruments
Venkataraman Srinivasan, Cirel Systems
Venkatesh Teeka, Samsung
Viji Ranganna, Qualcomm
Vinayak Agrawal, Intel
Wreeju Bhaumik, Analog
Zainul Charbiwala, Tricog

Keynote I

How AI is Changing the World of IoT

Shalini Kapoor - Distinguished Engineer at IBM, Director & CTO - Watson IoT and Watson Education at IBM

Shalini Kapoor is leading Mobile Enterprise applications Research at India Research Labs. She is building strategy and implementation around novel mobile solutions for Smarter Planet. Her research is leveraging mobile, speech, social networking, and context assets to improve urban and rural life. She is researching on needs and demands of mobile users and solutions spanning retail, healthcare, travel, banking and telco which will benefit citizens of the emerging countries.

She is a Senior Certified IBM Executive IT Architect. Prior to joining IBM she was working with the Strategy division of large services organization in India as an architect. She is Co Chair of Technical Experts Council and an ex-officio member of Academy of Technology. Shalini has done her B.Tech in Computer Science from University of Lucknow and MBA in Information Systems from S. P. Jain Institute of Management and Research, Mumbai.

SLIDES

Keynote 2

Quantum Computing

Dr.Susmita Sur-Kolay - Indian Statistical Institute, Kolkata

Susmita Sur-Kolay received the B.Tech.(Hons.) degree in Electronics and Electrical Communications Engineering from Indian Institute of Technology Kharagpur and the Ph.D. degree in Computer Science and Engineering from Jadavpur University India. She has been a faculty member in the Advanced Computing and Microelectronics Unit of the Indian Statistical Institute, Kolkata, India since 1999 and is presently a Professor. During the period 1993-99, she was a Reader in the Department of Computer Science and Engineering of Jadavpur University. Prior to that, she was a post-doctoral fellow at University of Nebraska-Lincoln, and a Research Assistant at the Laboratory for Computer Science in Massachusetts Institute of Technology.

She has served on the editorial board of the IET Computers and Digital Techniques, and IEEE Transactions on VLSI Systems. She is a Distinguished Visitor of IEEE Computer Society (India), Senior Member of IEEE, Member of ACM, IET and VLSI Society of India. Among other awards, she was the recipient of the President of India Gold Medal (summa cum laude) at IIT Kharagpur (1980), IBM Faculty Award (2009).

SLIDES

Tutorial 1

Chair: Garima Srivastava, Samsung

Functional Safety Trends: Challenges and Solutions

Trupti Joshi (Intel), **Ritu Agarwal** (Intel) and **Jaya Singh** (Texas Instruments)

Ritu Agarwal has been in Intel for 18 years playing various roles from Engineering management, SW Program Management both Pre-Silicon and Post Silicon programs for low power client and devices platforms. She's a certified PMP professional since 2005

Trupti Joshi is System validation expert and FuSa Validation Architect focused on Industrial and Automotive applications. In her 20 years career she has extensively worked on server core, PCI-Express, Ethernet & device safety mechanisms. She is certified Safety Engineer by TUV-NORD.

Jaya Singh is Engineering Manager at Texas Instruments India and have been with the organization for nearly 17 years, currently leading the C2000 microcontroller Design Group. Through her career she has gathered expertise in various areas of VLSI design covering the whole spectrum of a product cycle. She has been involved in several complex and challenging SoCs that make their way into automotive, industrial products focusing in functional safety.

SLIDES

Tutorial 2

Chair: Ranjini M, Texas Instruments

Using Cognitive Technologies for Improved Customer Experience

Gargi B Dasgupta (IBM)

Gargi B. Dasgupta is a Senior Technical Staff Member (STSM) and senior research manager at IBM Research, India. In her current role, Gargi is responsible for leading and contributing to innovations in the area of IT operational analytics - with an emphasis on cognitive solutions for optimization of IT infrastructure. She's done her Bachelors in CSE from Jadavpur University and PhD from University of Maryland Baltimore County. She has been with IBM Research for 14 years now and has 6 publications to her credit.

SLIDES

Invited Talk

Chair: Dr. Seema Chopra, Boeing

5G Evolution Concepts

Jiji Jayadevan and **Akshay Agarwal** (MediaTek)

Jiji Jayadevan is a Senior Department Manager at MediaTek and has been in telecom industry for 18 years playing various roles on engineering, management and research for 2G/3G/4G/5G physical layers.

Akshay Agarwal is a global leader with 19+ years of technical and business leadership experience in the US, Taiwan and India. He has played varied roles across engineering and research, marketing and business development, and organizational management.

Panel Discussion

Tracing the Trajectory of Women's Careers in Technology: Challenges & Solutions

Moderator: Antaash Sheikh (Texas Instruments)

Panelists: Krishna Paul (Intel), **Viji Ranganna** (Qualcomm), **Garima Srivastava** (Samsung) and **Roopashree HM** (Texas Instruments)

Background: While more girls are entering the engineering stream, this is not translating into higher representation of women in the workplace, and this disparity is more pronounced when we look at women in leadership roles in technology. The panel discussion will aim to throw light on what factors hinder women's careers in the technology space.

The topic covered four different phases of a woman's career and the unique challenges posed in each of these phases and suggested solutions. For solutions, companies can touch upon specific initiatives they've implemented along with other recommendations.

The four phases are – student of engineering, early career, break due to maternity, relocation or marriage, and post-break / second chance. While these problems are faced by women across industries, given the stats and representation of women in tech, it seems more acute within the tech industry. In keeping with the conference theme, we should try and link it to specific experiences of women in the tech field wherever possible.

Session 1.1 : Vehicular Electronics and Safety

Chair: Dr. Seema Chopra, Boeing

Paper: **12**

Design Approach for CCSDS Complied Command Operation and Frame Operation Procedure for Integrated Spacecraft Checkout

Parul Khurana, Sangeetha K. and Vithal Metri (ISRO)

Abstract: Consultative Committee for Space Data Systems (CCSDS) complied Telemetry and Telecommand Processor's (TTCP) development was taken up by Spacecraft Checkout Group (SCG) of U. R. Rao Satellite Centre, Indian Space Research Organization (ISRO) as a part of 'Make in India' campaign. As SCG is responsible for conducting exhaustive tests at integrated spacecraft level to evaluate and qualify the flight worthiness of subsystems onboard the spacecraft. This in-house Technology Demonstration/ Development of Consultative Committee for Space Data Systems (CCSDS) complied TTCP for spacecraft checkout applications in a cost effective and easy maintainable way, was taken up as a challenge. The in-house developed Processor was successfully deployed for the first time in checkout for Indian communication satellite and subsequently to Indian Remote Sensing (IRS) satellite. In future, TTCP will be used in Integrated Spacecraft Testing of ISROs Low Earth Orbit, Geostationary Orbit and Interplanetary Spacecraft missions.
The telecommand system plays a vital role in the success of any satellite mission. For effective control of various satellite subsystems, under all conditions, a highly efficient and responsive telecommand system is absolutely essential. This paper will brief about the design approach taken for implementation of CCSDS complied telecommand management and processing {Command Operation and Frame Operation Procedure (COP/FOP)} for TTCP developed by SCG.

PAPER … **SLIDES**

Paper: **73**

Information Extraction for Lightning Strike Related Aircraft Maintenance

Ankita Mathur, Halasya Siva Subramania and Micah Goldade (Boeing)

Abstract: Lightning strikes can cause extensive damage to an aircraft and affect both maintenance and safety operations. Understanding the effectiveness of current lightning protection and zoning in aircraft is essential; subject matter experts (SME) use this understanding to develop actionable threat mitigation strategies for improving design and developing efficient post-lightning strike repair specifications. We have proposed the use of data analytics in order to create a consolidated data source for lightning strike related events from maintenance logs. We have used a dictionary-based named entity recognition and dependency-graph based relationship extraction in order to extract most desired information from maintenance logs.

PAPER … **SLIDES**

Paper: **77**

Functional safety in Multicore Heterogeneous Systems for Automotive Surround view Applications

Vibha Pant, Piyali Goswami and Sujith Shivalingappa (Texas Instruments, Bangalore)

Abstract: Driverless cars are the next step in the evolution of the automotive industry. Advanced Driver Assistance Systems (ADAS) are the stepping stones to achieve and enhance the driving experience and more importantly safety in automotive systems. Safety standards such as ISO 26262 define Automotive Safety Integration Levels (ASIL) depending on the severity and probability of an error which may lead to loss/harm to life. Automotive electronic control units (ECUs) are made up of multi-core heterogeneous SoCs. Making all components of an automotive ECU to the highest ASIL level is not feasible due to significant cost and effort. This paper looks at software and hardware methods to have mixed safety levels co-exist in a heterogeneous SoC environment targeting surround view ADAS system while incorporating AUTOSAR requirements.

PAPER … **SLIDES**

HOME

Session 2.1 : System Design - 1

Chair: Chaitra Bhat, IBM

Paper: **18**

Unified Verification Methodology for Digital and Analog Mixed-Signal Co-Simulation for Low Power Embedded SoC

Ashwini Padoor and Lakshmanan Balasubramanian (Texas Instruments)

Abstract: Analog, power management and RF integration in a system on chip (SoC) require extensive focus on verification of analog design, system integration, low power intent, and use-case scenarios to ensure quality and timely product delivery. In this paper, we propose a unified environment and methodology for seamless verification of the mixed-signal SoC focussing digital, analog and low power aspects. The key features involve System Verilog (SV) Universal Verification Methodology (UVM) compliant architecture, reusable test bench and test case structure, common assertions and checkers.

PAPER … **SLIDES**

Paper: **44**

Design for Test Techniques to Enable Automotive Functional Safety

Swathi Gangasani, Prasanth V and Maheedhar Jalasutram (Texas Instruments)

Abstract: Periodic testing of electronic circuits in safety critical systems is becoming increasingly important due to the increasing safety and reliability requirements. Functional safety standards recommend targeted coverage goals to quantify the safety level for a device. Achieving these coverage goals using the traditional software based techniques is not practical. Adding redundancy to enable safety will result in significant hardware overhead. In this context, providing low cost (lesser area overhead, lesser impact on application MIPS, etc.) on-chip solutions to address field- test requirements is becoming increasingly important. These tests should be able to run in minimal time in idle slots of the application without affecting the application throughput. We should also ensure that there is no significant area overhead incurred in supporting these solutions on-chip. In this paper, we discuss various Design for Test techniques to enable application time self-test of various critical components of an SOC.

PAPER … **SLIDES**

Paper: **27**

Dimensionality Reduction for Handwritten Digit Recognition

Ankita Das, Tuhin Kundu and Chandran Saravanan (Jalpaiguri Government Engineering College)

Abstract: Human perception of dimensions is usually limited to two or three degrees. Any further increase in the number of dimensions usually leads to the difficulty in visual imagination for any person. Hence, machine learning researchers often commonly have to overcome the curse of dimensionality in high dimensional feature sets with dimensionality reduction techniques. In this proposed model, two handwritten digit datasets are used: CVL Single Digit and MNIST, and two popular feature descriptors, Histogram of Oriented Gradients (HOG) and Gabor filters, are used to generate the feature sets. Investigations are carried out on linear and nonlinear transformations of the feature sets using multiple dimensionality reduction techniques such as Principal Component Analysis (PCA), Linear Discriminant Analysis (LDA) and Isomap. The lower dimension vectors obtained, are then used to classify the numeric digits using Support Vector Machine (SVM). A conclusion arrived is that using HOG as the feature descriptor and PCA as the dimensionality reduction technique resulted in the experimental model achieving the highest accuracy of 99.29% on the MNIST dataset with the time efficiency comparable to that of a convolutional neural network(CNN). Further, it is concluded that even though the LDA model with HOG as the feature descriptor achieved a lesser accuracy of 98.34%, but it was able to capture maximum information in just 9 components in its lower dimensional subspace with the time efficiency of approximately 1/4th that of the PCA-HOG model and the CNN model.

PAPER … **SLIDES**

HOME

Session 2.1 : System Design - 1

Paper: **34**

22FDX Ultra Low Power Design with Dynamic Body Biasing and Liberty Variation Format

Suman Dwivedi, Ulrich Hensel, Chenbo Liu, Ramya Srinivasan, Siddhart Sawant and Haritez Narisetty (GlobalFoundries)

Abstract: In this paper, we are demonstrating how 22FDX dynamic body bias enables ultra low voltage design operating at nominal voltages of 0.4V, 0.5V, and 0.65V using the ULP_LV platform. Basic concepts of dynamic body bias for low voltage design are introduced. The necessity of Liberty Variation Format (LVF) deployment due to high local variations at worst corners under low operating voltages is discussed. We are detailing how LVF is used through the tool chain from library characterization to timing sign-off. The paper concludes with example block level implementation results.

PAPER … **SLIDES**

Session 1.2 : Wearables
Chair: Juby Jose, Intel

Paper: **93**

Short-term HRV using acceleration PPG under Severe Ambient Settings using in-house Developed Wearable

Payal Mohapatra, Preejith Sp and Mohanasankar Sivaprakasam (Indian Institute of Technology, Madras)

Abstract: The utility of heart rate variability (HRV) in clinical diagnosis, treatment of cardiovascular diseases, metric for social and mental well-being and physical fitness, is paramount. The gold-standard is to extract the variability information from the RR-intervals in ECG. Use of PPG as a surrogate to ECG have been put forth recently by many studies. In the presented work the use of wrist based PPG as an alternate to ECG for HRV is proposed. This would help in expanding the serviceability of wearable and portable heart rate monitors or simplify ambulatory monitoring of HRV. A novel optical sensor utilising yellow-orange emitters is designed to pick up optimal PPG signal from the dorsal side of the wrist using reflective plethysmography technique under no significant motion. The second-derivative approach is chosen to identify pulse intervals from PPG. The sensor and algorithm are validated on 5 subjects in particularly low temperature and high altitude conditions of Ladakh. Inspite of the potential setback due to the ambient conditions, on PPG acquired from the wrist, the optical sensor could pick up very good quality signals. The algorithm is also highly sensitive. Also the derived features and the intervals obtained from wrist-PPG are within a confidence of 5 % from that of ECG derived parameters.

PAPER … **SLIDES**

Paper: **47**

Indoor Positioning using Cellular Network and Relay node for Wearables

Sreelakshmi Gollapudi, Lalit Kumar Pathak, Tushar Vrind, Diwakar Sharma and Samir Kumar Mishra (Samsung Semiconductor India R&D, Samsung Electronics)

Abstract: One of the key requirements in public safety domain is to know the exact location of user or wearable device. There are a plethora of Internet of Things (IoT) based wearable devices which are getting used for geo-fencing and for alerting with position coordinates, but detection of indoor positioning is less accurate when is in basement/deep indoor. In Release 13, 3GPP defines architecture and solution to get near about indoor positioning using macro and small cells if GPS coordinates are not available. However, as the cells cover quite a big area, to improve the accuracy adding more small cells is a deployment challenge. Narrow Band IoT (NB-IoT) is a new specification proposed for IoT devices. One of the key proposition is to improve the coverage by 20dB to cater to basement/indoor. In this research work, we present our effort to use the NB-IoT nodes along with Device to Device (D2D) (relay based) technologies to get more accurate location by developing an algorithm to localize coarse and fine level proximity.

PAPER … **SLIDES**

Paper: **97**

Improved Network Analytics with Novel feedback Quantities for Self Optimized Networks

Roshni Chatterjee and Tushar Vinod (Samsung Semiconductor India R&D Cente)

Abstract: Self Optimizing Networks (SON) are emerging as the key component for cellular operators, and it is a big game changer for reduction in Operation and Maintenance (O&M) of the operators by automatically enhancing network performance, coverage and capacity. With the ever-increasing Capital Expenditure (CAPEX) required for newer technologies like New Radio (NR) to meet 5th Generation (5G) requirements, it is imperative for the operators to look at reduced O&M, as a way to optimize the Return on Investment (RoI) over several years. While SON is deployed in the recent times starting from 4G, after 3rd Generation Partnership Project (3GPP) standardized mechanisms like support of Minimization of Drive Test (MDT) logging in the User Equipment (UE), which suggests a continuous feedback based approach toward Network Analytics. In this paper, we propose schemes to add new dimensions to SON by incorporating novel measurement quantities in the MDT logging feedback, which serve to enhance the functionality of Network Analytics. The incorporation of measurements for 'battery drain rate', 'mobility state' and 'out of coverage cause' in the feedback can deliver substantial gain over existing feedback parameters.

PAPER … **SLIDES**

Session 2.2 : System Design - 2
Chair: Anjana Ghosh, Canon

Paper: **79**

Dual-Purpose Hardware Accelerator to implement a High-throughput FFT and Sorting Engine

Indu Prathapan and Pankaj Gupta (Texas Instruments)

Abstract: This paper describes a novel architecture for sorting binary numbers in hardware, based on a Radix-2 single delay feedback (R2SDF) architecture that is popularly used to implement pipelined Fast Fourier Transform (FFT) processors. The sorting algorithm used in this implementation is bitonic sorting. The spatial regularity of the bitonic sorting network and its similarity to FFT's signal flow graph (SFG) is exploited to map its comparator stages to the pipelined stages of the R2SDF FFT hardware with negligible area increase as compared to the original FFT engine. The data-path components like radix-2 butterfly units in a R2SDF FFT are replaced with 2-input comparators and some additional control logic for sorting engine. The proposed hardware accelerator can be configured by software to either compute FFT of N data elements or sort the N elements in linear order. For sorting N binary numbers fed into the proposed sorting engine in a serial order, a total of T(N*log2N) clock cycles are required. This is equal to the theoretical upper bound for sorting speed achievable with any comparison based sorting algorithm. The throughput of the serial hardware accelerator is further improved by 4x by increasing the parallelism in both the FFT engine and the Sorting engine. The proposed architecture is implemented in 45nm CMOS technology, meeting 400 MHz clock frequency.

PAPER … **SLIDES**

Paper: **94**

Dynamic Analytical Modeling and Optimization of Critical Healthcare Data using Connectionism Systems

Gagana B, H A Ujjwal Athri and Dr. Natarajan S (PES University)

Abstract: Classical Convolutional Neural Networks (ConvNets) have been the ruling benchmarks for most object classification and face recognition tasks despite major limitations such as the inability to capture spatial co-locality between data points and favoring invariance over equivariance mechanisms. Hence, Hinton et al, proposed a layered architecture called Capsule Networks (Capsnets) to overcome these shortcomings by replacing pooling techniques with dynamic routing abilities between lower level and higher level neural units which better capture hierarchical relationships within the data, thus, outperforming traditional systems. By overcoming existing limitations, Capsules have proven themselves to be potential benchmarks in object segmentation, detection and reconstruction. Capsules have achieved state-of-the-art results on the fundamental MNIST dataset by reducing the ConvNets test error benchmark of 0.39% to 0.25%. The two novel aspects inspected in this paper are the augmentation of this error benchmark distinction by optimizing the architecture through five activation units such as sigmoid, e-Swish, Swish, variants of Rectified Linear Units (ReLU) like Parametric ReLU (PReLU) and Scaled Exponential Linear Units (SELU) and the applicability of results obtained on visual data to stochastic numeric healthcare data uncovering newer challenges of predictive neural networks.

PAPER … **SLIDES**

Session 2.2 : System Design - 2

Paper: **83**

Divergence Engine: Early prediction of Clock-tree Divergence at Logic-synthesis Stage

Sanjana Sundaresh, Murali Mohan Thota and Atul Garg (Texas Instruments)

Abstract: Timing convergence, while reducing area and power, is one of the hardest challenges in the physical design of nanometer VLSI chips which push the limits of frequency entitlement. If there is clock tree divergence (CTD) due to architecture in a high frequency design, then margins are required during optimization stage. These margins will account for divergence at the early stages that can significantly impact the frequency entitlement. However, each timing path can have different divergence values and applying the same margins across all paths is not optimal. To address CTD, applying flat margins can lead to incorrect frequency entitlement, impacting area and power. If accurate path specific margins based on CTD are used, it will help in early optimization stages i.e. at logic - synthesis and placement to achieve the right power, performance, area and schedule (PPAS). Early identification of critical paths which are highly clock tree divergent at logic-synthesis stage and in-time architecture feedback will go a long way to reduce design or project cycle time.

PAPER … **SLIDES**

POSTER PRESENTATIONS - 1

Poster: **30**

Effect of Performance on Containerized Deep Learning Applications

Vinutha Gs and Anto Ajay Raj John (IBM India Pvt Ltd)

Abstract: The advent of machine learning, deep learning has brought in a paradigm shift on workloads running on server systems, with the heavy cost associated with running them on superior hardware. In the application-development and cloud deployment domain, containers have become the cynosure of all the developers. Containers come with a low overhead, provide increased distributed computing capabilities and reduced complexity by abstracting away application dependencies. Thereby, containers provide for easier application sharing, migration and cloning, by clubbing the application and its development environment into a single component. Deep Learning(DL) frameworks have many dependencies and it has a rapid development cycles and changes. Containerization helps developers overcome these challenges and therefore are rising in importance with deep learning frameworks.

In this paper, we compare the performance of native versus containerized Deep Learning applications using deep bench and fathom benchmarks. These two benchmarks almost cover all the aspects of deep learning computation from a micro and macro application level. Deep bench identifies fundamental operations in Deep Learning applications like gemm, reduce etc. and evaluate the same; while Fathom provides a collection of deep learning workloads built around Tensorflow covering the spectrum of current deep learning applications like Convolution neural network, Recurrent neural network, etc.

We have demonstrated that except for a few aspects of performance differences; largely containers prove to be a great platform to package and host deep learning applications.

PAPER … **A3 Poster**

Poster: **33**

Implementation of Speech Recognition on Edge Devices

Shaik Shabana and Sujith Thomas (Intel)

Abstract: In Today's World, Deep Learning and Artificial Intelligence are changing the way we approach and resolve Life's Problems. With the advancements in Neural Networks, the scope for Deep Learning based solutions is widening. Edge Computing is taking the World by Storm penetrating into segments never thought off. Implementing Speech Recognition on Edge devices using Deep Learning techniques gives a wider foray to businesses to accelerate the processing power of hardware and leverage the user experience. This paper explains the challenges, techniques and provides an insight in the implementation of speech recognition models on Edge Devices. Edge Devices with Android as the Operating System is taken as platform to analyze the problems and to quantify the benefits of such this implementation. This paper also showcases the process to integrate and enable speech model for on device inferencing on Android Devices. Proposed Method is unique in its way because of two reasons. Firstly, it opens the doorways of on device inferencing with the help of neural network API's (NNAPI's) which can eliminate more resources, costs, time needed for cloud based inferencing, promote secure control of data, and leverage user experience in no time. Secondly it demonstrates the performance impact of the Android Runtime HAL on NNAPI's. There is very little research on deploying speech recognition on Android for edge devices and using the Android neural network runtime to accelerate the processing and quantifying the performance impact. This research is aimed at developers who can deploy speech recognition at low cost and with ease enable speech recognition for their projects.

PAPER … **A3 Poster**

POSTER PRESENTATIONS - 2

Poster: **39**

Context aware Methods for Uplink Centric NBIoT Devices

Meha Goel, Tushar Vrind and Diwakar Sharma (Samsung Semiconductor India R&D Center, Bangalore)

Abstract: Cellular communication is a great enabler for Internet of Things (IoT), as it offers coverage, quality of service and most importantly the maintenance and operations is centralized and taken care by the operator. Narrowband IoT (NB-IoT) is designed by 3rd Generation Partnership Project (3GPP) for a plethora of use cases which cater to broad spectrum of capabilities but introduces few in-efficiencies in the resource allocation and adds overhead in the system. We envisage a use case aware NB-IoT network, which creates opportunities in the system for dynamic adaptation of the resource allocation for NB-IoT devices. We present protocols and algorithms both on the network and device side suitable particularly for 3GPP NB-IoT deployment. This demonstrates over 90% improvement in the power consumption (through removal of DRX and measurements), lowers RACH overhead during device admission (through context based cell search) and improvement in reliability during emergency scenarios. Thus, the proposed solutions enable use cases for activity tracking and emergency reporting within the latency budgets, improving user experience and battery life for NB-IoT devices in the field.

PAPER … **SLIDES**

Poster: **41**

No reboot Operating System Update using OpenStack Technologies

Sanchita Sinha (IBM India Pvt Ltd)

Abstract: At Several occasions there might be need for Operating System to upgrade itself by installing bug fixes (Kernel, Kernel Extensions) or by moving to a newer Service Pack. This affects business critical workloads as the system needs a reboot for the newer version to take effect. This issue can be solved by using the live update operation which allows the application of bug fixes and Services Packs without requiring a system restart.

This paper will provide an insight on different challenges and requirements needed for live update operation and how one can leverage the OpenStack Technologies to overcome those.

To Perform live update operation, one major challenge is the admin effort to setup the environment. This paper will provide a detailed insight into how OpenStack technologies provide solutions to resolve the challenges, greatly reduce manual effort and provide cost effective solutions.

PAPER … **SLIDES**

Poster: **42**

Real Time Memory Regeneration in Constrained Embedded Systems

Lakshmi Prasanna Jasti, Kashmira Kapoor, Tushar Vrind, Diwakar Sharma and Raju Udava Siddappa (Samsung Semiconductor India R&D Center, Bangalore)

Abstract: Embedded devices are mostly used in products where amount of available memory is limited and often we encounter situations where the installed user applications end up consuming more memory than designed for; which is reported as a system failure. The memory requirements of the embedded system's applications frequently overrun the initial estimates & could lead programmers to over budget the memory usage easily by over 20%. We discuss a software based novel approach which can be deployed in a Real Time Operating System (RTOS) for an embedded processor, which does not have a demand paged and virtual-physical address translation architecture (Memory Management Unit (MMU)-Less). In this paper, we propose the algorithm to be adopted by the RTOS Scheduler, which finds the transient unused block of memory to be compressed, and allocates the remainder block to the task which may need additional stack or dynamic memory. The proposed algorithm discusses the steps of compression, decompression and management to utilize the regenerated memory. With this optimizations, we can regenerate memory dynamically (theoretically to almost double) and system failure rate can be improved based on above probability improvement.

PAPER … **SLIDES**

POSTER PRESENTATIONS – 3

Poster: **43**

Application specific Transmit Power Optimization using Predictive Modelling

Hinduja Ichapuram, Prasad Rao, Maulik Patel, Diwakar Sharma and Tushar Vrind (Samsung Semiconductor India R&D Cente, BANGALORE)

Abstract: The ever changing nature of a User Equipment (UE)'s channel conditions pose a challenge to the existing closed loop power control technique. Today, most of the power control algorithms are highly dependent and controlled by the feedback and indications provided by the UE resulting in power hungry Radio Frequency Integrated Circuit (RFIC) component operations. This paper aims at deferring and optimizing Long Term Evolution (LTE) Transmit (TX) power for background data by reducing the RFIC's power consumption. Further, a predictive algorithm is used to determine and schedule TX at an optimal power level. This idea also finds application in low power distributed wireless sensor networks/IoT

PAPER … **SLIDES**

Poster: **48**

Automated Log Analysis in Communication Systems

Divjot Kaur, Roshni Chatterjee, Rajdeep Kaur and Surendra Singh (Samsung Semiconductor India R&D)

Abstract: Modern smartphones, servers, routers and other products have complex components, which interact with each other using different protocols. More than a billion such products are sold each year- so it is a herculean task for the different companies involved in the development and sales of such products to ensure that the products work flawlessly without any anomalies. Therefore, any new model of such products must undergo exhaustive testing globally before it can be launched. These wide range of tests generate a huge amount of logs.

Analyzing these logs manually is a mammoth task. It takes a lot of man-hours across different test sites. This affects the turn-around time required to identify and fix issues. To solve these problems, Automatic Log Analysis needs to be implemented to reduce the burden of analyzing the logs manually, identifying issue logs efficiently, and assigning the issues to right developers, so that developers can focus on fixing the issues rather than having to go through thousands of logs, which may or not have any relevant issue scenarios.

With the recent advancements of supervised machine learning methods, training the computer to perform offline and online log analysis is possible within this industry.

PAPER … **SLIDES**

POSTER PRESENTATIONS - 4

Poster: **54**

System Optimization for Enabling Debugging

Anudhi Jain, Raju Udava Siddappa, Tushar Vrind and Venkata Raju Indukuri (Samsung Semiconductor India R&D Center, Bangalore)

Abstract: Embedded systems are designed with low on-chip RAM and low processing power to reduce cost and power consumption, so software running on it should be optimized to utilize less resources. At the same time it is important to allow room for adding debug information so that failures can be analyzed quickly in order to reduce overall software development cost. Usual methods of adding debug logs in a software has both memory and performance overheads. In this paper we discuss mechanisms through which the debug log mechanisms memory overhead can be reduced by nearly 100%, and its processing overhead can be reduced by over 85%. Through this optimization it is expected that the development cost will be reduced, and in addition it will improve the systems scalability to meet future incremental requirements.

PAPER … **SLIDES**

Poster: **87**

Comparison of Diagnostic Machine learning Models with Physics based Models for Predicting the Lithium-ion Battery Degradation Behavior

Akshata Kishore Moharir, Srishti Gautam, Seema Chopra and Naveen Kumar Megharaj (Boeing India private limited)

Abstract: A novel data driven approach is developed for predicting the battery degradation behavior for lithium-ion batteries using Regularized Greedy Forests (RGF). The aim of this novel approach is to improve and compare the prediction accuracy of the lithium ion (Li-ion) batteries using physics based models and surrogate models which are machine learning (ML) models. First, the approach takes in state of charge, state of health, and power of the battery as inputs and predicts the solid electrolyte interface of the Li-ion batteries which lead to the capacity fade which can be the additional cost of batteries. Second, the RGF is proposed as the new ML regressor for failure diagnostics to determine the battery degradation behavior.

The prediction is based on the assumption of the availability of real-time observation and historical data. The feasibility of the regressors is validated using Li-ion battery diagnostic data. The experimental results show the following: (1) Fewer data dimensions for the input data are required compared to traditional state-of-art ML models (2) Physics based models describe the battery behavior accurately but they are computationally costly, therefore we have developed surrogate ML models for physic based models which are cost effective (3) The proposed ML regressor provides an effective way of diagnosing battery degradation behavior of the Li-ion battery compared to state-of art Surrogate ML algorithms with small error and has high prediction accuracy.

PAPER … **SLIDES**

DEMO - 1

Demo: **2**

Time Sensitive Networking over WiFi

Ritu Sethi and Dave Cavalcanti (Intel)

Abstract: Time Synchronization capability over WiFi networks is a new feature which attempts to reduce the latency of WiFi transmissions for time sensitive applications which require its tasks to be completed in a deterministic and timely fashion. The main applications revolve around the following domains - Autonomous Systems, Industrial Automation and Immersive VR Gaming.

This demo leverages the Wireless Time Sensitive Networking concepts to achieve tight time co-ordination between configured WiFi devices. When WiFi devices co-ordinate with each other in time, it makes possible lesser contention for the access of the Wireless medium. This also allows the WiFi devices to use the spectrum more effectively as they now co-ordinate with each other before trying to access the medium.

The demo showcases a Kinematic Control system comprising of a ball and a balancing board controlled by an X and Y Position Servo Motor and 2-D resistive touch sensor. The touch sensor provides 2-D feedback to the controller which then drives the servo motor in a controlled loop. The demo showcases the manual mode of operation where user sends commands to control the servo motor wirelessly. It is seen that Latency of the communication link and reliability of packet transmission have a direct impact on user's ability to control the system. Large latency results in excessive lag in the system which results in degraded stability and user experience. The original control system has all wired communications. In this demo this wired link between the user controller and the balancing board controller is replaced with 802.11ac wireless link. The three modes of operation presented are - Wired mode, Low latency WiFi mode and a High/Variable latency WiFi mode to clearly show the user experience in each mode and the comparable user experience in Wired and Low latency WiFi mode.

SLIDES … **A3 Poster**

Demo: **82**

Occupancy Detection and People Detection on an Edge Device for Smart Building Automation

Linet Paul and Raka Singh (Analog Devices)

Abstract: Automation of buildings for energy efficiency, space utilization and increase productivity of workplaces through measurement and control of several parameters such as temperature, oxygen flow, HVAC control is becoming important. Hence people counting and occupancy detection are important sensing parameters, since people detection and occupancy detection can drive space utilization in buildings, optimal use of energy for HVAC, Oxygen monitoring. For privacy and security and data bandwidth limitations, the data cannot be streamed to the cloud. Hence the detection has to be done an edge device, at accuracies of 90%+, with a single device having a coverage area of 30 sqm.
We propose an imager based solution, with a low power, high performance ADSP-BF707 400 MHz Blackfin DSP, with the video being analysed on the edge device using computer vision and machine learning algorithms. Our solution is an end-to-end solution, where the metadata is send to the cloud on WiFi, and the data is analysed on cloud to enable business analytics for the end user. The main innovation in our solution are the algorithm blocks which gives us a 90%+ accuracy on a VGA resolution 10 fps video, easy to use commissioning of the device from Mobile App, over the air upgrades, and a flexible and scalable architecture for the framework.

PAPER … **SLIDES**

DEMO - 2

Demo: **99**

PPG and ECG Signal Generator to Automate System and Algorithm Validation

Shabana Yerragudi and Nayan Bhatt (Analog Devices Pvt Ltd)

Abstract: ADI's ingenious biopotential generator are extremely helpful for testing and validating various algorithms at system level and module level. These simulators are extremely helpful in testing sensors and algorithms validations for their functional and non-functional conformation with specific requirements and for different system level use cases which are not always practical due to lack of availability of test subjects (humans).
ADI's Signal Generator also provides functionality to change the cardiac cycles pattern to represent regular and irregular patterns at variable rate from 40 to 240 bpm.

PAPER … **SLIDES**

Demo: **100**

Assisted Car Exit using RADAR

Saranya Das and Sriram Madavswamy (Analog Devices Inc)

Abstract: Car Dooring is when the door of a car is carelessly opened and it hits an incoming vehicle and this is serious problem for which automotive companies are looking for a solution. This type of sudden crash may eject the rider from their bike and lead to fatal injuries. We are trying to solve this problem via a RADAR based solution. Our solution benefits car users by not only preventing damage to their cars but also preventing potential accidents with fellow bike riders and pedestrians. To demonstrate this, we are using ADI's 24GHz Demorad platform.

PAPER … **SLIDES**