IEEE WINTECHCON-2019

Technical Conference by Women Engineers … 27 September 2019 … Bangalore

Updated: 16 October 2019

Organized by: IEEE CAS Bangalore Chapter
In cooperation with IEEE WiE Council
(IEEE Women in Engineering), Bangalore

and

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Conference Proceedings

IEEE WINTECHCON - 2019

Technical Conference by Women Engineers
27 September 2019 … 8AM to 5PM
HOTEL SHERATON GRAND, Whitefield, Bangalore

Objective: *To provide opportunities to women technology leaders from India to present their work in emerging knowledge areas*

Theme: **Future Technologies for a Smart, Safe and Sustainable World**

About WinTechCon-2019
Reviewers (3, 4)
Keynote & Panel discussion

Presentations

Track 1.1 : **VLSI Design and Test-1**
Track 1.2 : **VLSI Design and Test-2**
Track 2.1 : **System Optimization-1**
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Poster papers

Posters Papers (10, 11, 12, 13)

Demo projects
Hackathon

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About the Conference

Over 400 women engineers from 35 organizations gathered at Bengaluru for the IEEE WinTechCon 2019 conference, with the theme "Future Technologies for a Smart, Safe & Sustainable World". This was the second edition of the annual technical conference organized by senior women technologists, in partnership with IEEE CAS (Circuits & Systems Society) Bangalore Chapter, IEEE Bangalore Section and IEEE WiE (Women in Engineering) Council Bangalore.

The day-long program was the culmination of several technical tracks – the conference received over 200 manuscript submissions from women engineers and students, of which **18 papers were selected for presentation** at the conference. In addition, **14 posters** and **9 demos** were showcased. These covered technology areas spanning VLSI Design and Test, System Optimization and System Software and AI. The IEEE WinTechCon 2019 also featured a hackathon with hardware and software tracks, with finalists showcasing their projects at the conference.

The academic track featured tutorials on topics including *Automated Driving – from ADAS to Driverless Cars*, to *Open Source Technique for Large Deep Learning Model Training* and *Emerging Trends in WiFi*.

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Keynote talks

Keynote-1:

AI-enabled Healthcare for the Masses

Dr. Geetha Manjunath, Co-founder & CEO, Niramai

Use of Artificial Intelligence based tools in clinical applications will make healthcare more accessible, affordable and scalable to the masses. NIRAMAI is attacking one of the largest cancer killers among women today. AI is now ready for life saving applications. It really works.

She said *"It is heartening to see this conference that was conceptualized and started last year become twice as big and impactful. The steering and technical program committees comprise leaders from across the VLSI, EDA and R&D space. The purpose of the conference is to provide a platform for women technologists and we are encouraged by the huge response we have seen."*

SLIDES

Keynote-2:

Journey of Intrapreneurship

Reena Dayal Yadav, Director, Microsoft Garage-India

She said "Innovation is about taking risks, one needs to be prepared for failure as much as look forward to success. We drive a culture of learning and innovation within Microsoft to enable ideas to germinate, we are customer obsessed and connected to customer needs, we provide a safe place for people to take risks with their ideas, to fail and then to succeed. I congratulate IEEE WIE team and the semiconductor industry teams to have organized this event and for raising the bar on the dialogue with women engineers."

SLIDES

Panel discussion:

What Drives Me – Strategies and Taccs for a Technologist's Career

Moderator: *Roopashree HM (Texas Instruments)*

Panelists: *Jiji Jayadevan (Mediatek), Seema Chopra (Boeing), Piyali Goswami (Texas Instruments), Upma Sharda (Qualcomm), Shyama Venugopal (IBM)*

Track 1.1: VLSI Design and Test-1

Session Chair: Ritu Singh, Texas Instruments

Regular Paper: R**46** … Best Paper Winner (Hardware)

Optimized Battery Life for Ultra-Low Power Products

Shweta Aladakatti, Jasdeep Jain, Shubham Singh, Narayanan Natarajan, Purna Nayak and Yojak Raote (Intel India Tech Pvt Ltd)

Abstract: "The urge for devices with longer battery life in today's compute world has motivated multiple changes in the design, architecture, and SW optimizations. Ultra-Low Power products [Mobiles, Tablets, Notebooks, and Convertibles] are constrained by 2 major factors – thermal dissipation and supply of battery power. Thermal dissipation restricts power consumption of application processor, which additionally limits computational performance. Battery usage time is determined by power consumption of the device. Due to these reasons, power management to improve efficiency of electric power usage becomes a very crucial part of ULP products. Battery life suite is introduced with real time use cases or KPI's to analyze battery life of the product. This paper presents the optimizations that were developed for improving the battery life performance of ULP SoCs. The use cases/KPI's defined in BL suite were used as metrics to evaluate the features. We present the features in two categories spanning architecture and software optimization. A detailed power modeling exercise was undertaken for evaluating the features, including detailed model correlation with post-Si data from previous generation products. The combined benefit of the features translates to an overall improvement of ~34% SoC power and ~11.5% increase in battery life for suite i.e. ULP product is very close to the target of maintaining the hours of battery life expected by the suite. These features have been adopted by products across several segments."

PAPER … **SLIDES**

Regular Paper: R**62**

Validation methodology for Nest Memory Management Unit

Nandhini Rajaiah Jayakumar N Sankarannair (IBM Bangalore,India) and Larry S Leitner (IBM Austin, United States)

Abstract: "The growing demand for performance makes the processor logic design more complex, thereby making post-silicon validation a critical and complex step in processor development life cycle. There are complex units with newer timing and control logic paths which are almost impossible to exercise in regular verification environments. One such unit to cater to newer workloads in recent superscalar processors is the Nest Memory Management Unit (NMMU), a memory management unit for all I/O devices. This paper presents some of the major challenges in validating Nest MMU. A post-silicon validation framework is proposed to mitigate these challenges. An asynchronous non-blocking accelerator job submission model is used in this approach to increase the translation traffic from the agent to NMMU. Core MMU translation is used as the reference model to validate nest MMU. The processor core storage exception handlers are leveraged to minimize the validation tool software development effort and to increase the efficiency of validation as well. This method makes use of an optimized threshold-based checker to detect potential NMMU hardware issues. The proposed methodology has been experimentally evaluated in Power9 NMMU to demonstrate the effectiveness of the method in providing considerable stress to the unit."

PAPER … **SLIDES**

Regular Paper: R**117**

Design and Verification Challenges with Third Party IP Cores

Ruchi Shankar, Prachi Mishra, Abhinav Parashar, Ashwini Padoor and Lakshmanan Balasubramanian (Texas Instruments India)

Abstract: "IP reuse is all about improving productivity and can result in significantly shrinking the design cycle time especially with configurable third party IP cores. Increasing amount of third party IPs find their way onto today's complex system-on-chip (SoC) designs. Hence it is paramount that designers build a large and expanding knowledge base incorporating lessons learned out of accumulated experience from several of designs containing a broad range of IP blocks into tangible design, verification and test methodology components. These components include checklists, automated IC analysis programs, and processes both internal and collaborative. This knowledge base is usually combined with the experience of the individual IP and EDA vendors to ensure the lowest possible risk to each design. Integrating third party IP core typically involves various challenges. These challenges involve compatibility with power, reset and clock (PRC) schemes, design methods used to achieve system low power goals, integration scalability, and design verification methods to achieve comprehensive entitled coverage. Resolving them requires additional design, integration and verification effort. Design verification (DV) in general could be more challenging, as most third party IPs are verified in isolation agnostic to the context of the system. Ensuring that the third party IP cores as used in the SoC will ultimately meet all requirements is a highly complex task that requires a dedicated, expert team with an explicit focus and responsibility towards this task. This paper outlines design and DV challenges and resolution in integrating third party IPs in today's high-end ASICs/SoCs"

PAPER … **SLIDES**

Track 1.2: VLSI Design and Test-2

Session Chair: Garima Srivastava, Samsung

Regular Paper: R**69**

Automation of Verification for Application Specific Instruction Set Processors

Sreenivas Machavaram, Chaithanya Kolikipudi, Tal Milea and Parakalan Venkataraghavan (Intel Technology India Pvt. Ltd.)

Abstract: "Application Specific Instruction-Set Processors (ASIPs) achieve high performance and flexibility by using specialized instructions implemented in C-programmable custom hardware functional units (FUs). Typically, the instruction set is formally represented in a high-level language like C and custom hardware is implemented in RTL with several optimizations necessary for practical silicon implementation (e.g. resource sharing, pipelining). Verifying functional correctness of the RTL implementation through an automated process is a challenging task. In this paper, we describe an automated framework developed for constrainedrandom functional verification of custom FUs for an application-specific SIMD processor with n-bit (n in order of 1000's) wide data-path which has been instrumental in finding RTL bugs. We are currently working on extending this process to use formal techniques for more comprehensive data-path verification."

PAPER … **SLIDES**

Regular Paper: R**74**

HVDM Solution for Random Verification of Microcontroller based Subsystems

Ruchita Pathak, Aravind Bhat and Vishalkumar Dewan (Chipset and IP technologies Group) Intel Technologies, Bangalore, India

Abstract: "A typical microcontroller based system often includes multiple interfaces with an ability to support clock gating and other low power features. For such a complex subsystem, finding issues in block level interaction, low power flows and architecture requires exhaustive random test framework at subsystem level along with unit level randomization. There is no standard approach for developing random verification environment for such subsystems, thus resulting in increased time for development and maintenance. Debugging issues wherein concurrent traffic from different interfaces is active, is challenging and time consuming. In order to support multiple projects with different configurations there is need for scalable and structured approach which would help in achieving quality verification without affecting time to market. A novel dashboard style architecture proposed in this paper, provides fully scalable solution for subsystem level random verification with improved debug ability and execution efficiency, thus contributing to High Velocity Development Model (HVDM). With this scalable approach for random verification, bring up time for a new IP in a Sub system random verification environment is seen reduced by 60% and time required for achieving tape-in quality coverage is seen reduced by 40%, as compared to the traditional approach. The results published are derived from the improvement seen by implementation of this methodology in a Low Power Sensor Subsystem that was delivered to multiple SoCs, in time with quality."

PAPER … **SLIDES**

Regular Paper: R**104**

A Generic Layout Automation Model to Achieve Minimal Time-to-Market

G S Aishwarya Meghana, Sheetal Y Kochrekar and Poornima Venkatasubramanian (Samsung Semiconductor India R&D Center) Samsung Electronics Bangalore, India

Abstract: "With the ever growing demand for IPs in the domain of mobiles, 5G, and sensors for wearables and for applications, time to market becomes a crucial factor. There is always a need for delivering IPs to the competitive market in very less time without compromising on the quality. This necessitates the development of a reliable automation technique that can be easily integrated into the design cyelc and Quality assurance flog of an IP. In this paper, we propose a generic automation flow for generating seed layouts for any technology node. The proposes new redness manual affirm and Imnmves overall productivity."

PAPER … **SLIDES**

Track 2.1: System Optimization-1

Session Chair: Manoj Choudhary, Samsung

Regular Paper: R**146**

Novel Pulse Width Insensitive Design and Verification Methods

Ruchi Shankar, Shalini Eswaran, Sharavathi Bhat and Lakshmanan Balasubramanian (Texas Instruments India)

Abstract: "Many embedded controllers have some critical system states that depend on an asynchronous event. Currently handling them in design depends on the availability of always-on slow clocks. In this paper we present a generic asynchronous design scheme that doesn't require a clock and ensure a reliable functionality without associated deadlock scenarios sensitive to exact arrival times of asynchronous events. This is enabled by a novel pulse width insensitive design method, which also requires unconventional verification methodology that ensures thorough and comprehensive presilicon design quality. These have been applied on the latest, ultra-low cost embedded micro-controller design targeted for cost sensitive applications."

PAPER … **SLIDES**

Regular Paper: R**34**

Novel Infrastructure Design for multi-FPGA Prototyping system

Vandana Singh, Ranjith Kulai, Vani V and Gregory Matthew James (Intel Corporation Bangalore,India)

Abstract: "In a multi-FPGA based prototyping, an SoC is partitioned into multiple modules. Each FPGA contains a partitioned module in addition to FPGA specific infrastructure components. The functions of these components are to generate clocks, to multiplex interconnect signals and to interface with peripheral components. The handling of a multi FPGA system in the engineering process is challenging task. It requires comprehensive knowledge of system architecture, specification of FPGA device used and hardware definition languages. In this paper, we propose a 'plug and play' framework which aids in seamless stitching of partitioned module with FPGA infrastructure. An FPGA has limited resources for logic implementation and routing. These infrastructure components are overhead to implementation of the desired partitioned module. This paper discusses a novel infrastructure design which is scalable, robust and reduces turnaround time. Additionally, this paper also presents a scheme for pin aware placement TDM components that can address routing congestion."

PAPER … **SLIDES**

Regular Paper: R**118** … Best Paper Runner-up (Hardware)

Integrating Functional Safety in AC/Servo Drives with Redundancy and Diagnostic Coverage

Aishwarya Bhatnagar, Vaibhavi Shanbhag and Navaneeth Kumar (Texas Instruments)

Abstract: "Functional safety has become an integral part of motor drives. The main objective of functional safety is to bring the machine to a safe state quickly. A fail-safe system is fault-tolerant and inherently responds in a way that causes no or minimal harm to the machinery and operator. This paper presents the method of implementing safety functions defined in IEC-61800-5-2 like Safe torque off and Safe brake control. It also shows implementation of Safe power supply and Safe digital I/O to be integrated in the power converter for achieving high safety standards. These implementations not only add redundancy but also facilitate diagnostic coverage. The solutions proposed in this paper are validated under different test conditions."

PAPER … **SLIDES**

Track 2.2: System Optimization-2

Session Chair: Saritha Vinod, IBM

Regular Paper: R**136**

Cross-Layer Optimized MBMS Performance for DSDS User Equipment

Krishna Daamini Ellendula, Vinay Kumar Shrivastava, Lalit Kumar Pathak and Rohan Raj (Samsung Semiconductor India R&D Center) Samsung Electronics Bangalore, India

Abstract: "Multimedia Broadcast Multicast Service (MBMS) primarily targets broadcasting mobile television contents and video streaming services. Consumers worldwide are rapidly using Dual SIM Dual Standby (DSDS) device that utilizes a single common Radio Frequency Integrated Circuit (RFIC) for supporting more than one Subscriber Identity Module (SIM) cards. These two popular feature requirements are quite contrasting and pose a significant challenge to the design and implementation of User Equipment (UE) to achieve lossless MBMS video performance and Call connectivity Key Performance Indexes (KPIs). This Paper, to the best of our knowledge, first time provides a cross-layer optimized approach merging the “application-domain” quality metrics to the modem level realization of the DSDS RFIC scheduler algorithm and enhances the performance. Based on the mathematical modelling supported by simulation results, proposed algorithm provides the guidelines for designing the RFIC scheduler for DSDS operation."

PAPER … **SLIDES**

Regular Paper: R**138**

Novel Approach for Prioritization of TCP Acknowledgements in Beyond 4G and 5G network

Lakshmi Prasanna Jasti, Rohit Kumar, Tushar Vrind and Lalit Pathak (Samsung Semiconductor India R&D Center) Samsung Electronics Bangalore, India

Abstract: "Evolution in cellular wireless communication and standardization has brought out technological advancements in physical and medium access (MAC) layer protocol to scale the data rate on the air interface like in Long Term Evolution (LTE) or New Radio (NR) 3GPP standards, by 10X to 100X compared to older technologies. At the same time there is not much thrust given on the interworking with TCP/IP, resulting in poor user experience, as a similar scale of improvement is not seen at application level, once the technologies are deployed in field. The problem related to delayed TCP acknowledgement (ACKs) acts as bottleneck at application level, which in turn results in low uplink (UL) or downlink (DL) Throughput (TP) at the User Equipment (UE). Solutions available in the literature to address the same increase either the processing complexity or wastage of resources, or both. In this paper, two novel solutions are presented to address prioritization of TCP ACKs by Sequence Number (SN) reservation and SN space management in simultaneous UL/DL traffic scenarios while maintaining low complexity. Through mathematical modelling and simulation in a standard setup for LTE network, we are able to achieve the effective decrease in downloading time by 5 ~ 25% in comparison to standard schemes. The solution is easy adoptable in NR based 5G network"

PAPER … **SLIDES**

Regular Paper: R**167** … Best Paper Runner-up (Software)

Kernelization of Vertex Cover Based on Crown Structure

Divya U (Intel Technology India Pvt. Ltd.)

Abstract: "Kernelization is the technique of preprocessing a problem instance to reduce it to a smaller instance. In this paper we discuss the kernelization technique for a graph problem called vertex cover. This technique is based on a graph structure known as crown structure. The current best known solution for kernelization of vertex cover based on crown structure reduces the problem instance to a smaller instance of size 3k, where k is the size of vertex cover. The solution discussed in this paper reduces the problem instance to an instance of size 2k. Vertex cover has applications in computer network security(worm propagation) and machine learning(text summarization)."

PAPER … **SLIDES**

Track 3.1: System Software and AI-1

Session Chair: Raka Singh, Analog Devices

Regular Paper: R**131**

Automatic Defect Classification and Localization of MURA Defects

Ramya Bagavath, Gaurav Sultania, Gaurav Kumar, Shashank Shrikant Agashe, Priya Ranjan Sinha (Samsung Semiconductor India R&D Samsung Electronics Bengaluru, India) and Chulmoo Kang (Mechatronic R&D Center Samsung Electronics)

Abstract: "MURA defects in LED/LCD panels are one of the most challenging defects for Automatic Defect Classification and Localization (ADC) due to their extremely low contrast with compared with the background. Manual detection is subjective, error prone, very tedious and time consuming. Even when the type of MURA defects can be ascertained manually the exact bounding box for defect is hard to determine. Various heuristic based image processing technique have been applied giving sub-optimal accuracy over generic datasets. Moreover for each defect, type different processing pipeline had to be designed. In this paper we present a single DL pipeline for classification and localization, which is first of its kind for MURA defects. Using optimization techniques that are from both DL field as well as specific to MURA domain, we show improvement in the accuracy of the base DL pipeline from ~30% to ~80%."

PAPER … **SLIDES**

Regular Paper: R**133**

Uplink Data Compression for futuristic wireless networks

Shalini Govil, Rohit Kumar and Pavan Kumar Devarayanigari (Samsung Semiconductors India R&D Centre), Samsung Electronics, Bangalore, India

Abstract: "3GPP Uplink Data Compression (UDC) improves the network resource utilization, reduces transmission time during high data transfer and improves user experience in poor signal condition. The paper discusses the issue of UDC packet loss arising due to UDC checksum failure as well as the limited scope of UDC interworking along-with new 3GPP features like PDCP duplication, RLC Out-of-Order delivery, Split bearer in dual connectivity and PDCP discard timer for effective QOS maintenance. The paper proposes a novel method to enhance UDC support across new 3GPP features. It also proposes two methods; a preventive approach and a recovery approach for handling packet loss issue. In our simulation on LTE test bed, method one saves 50% of network resources and recovery method recovers all UDC packet losses."

PAPER … **SLIDES**

Regular Paper: R**165**

Edge Acceleration of Computer Vision and Deep Learning Algorithms using OpenCL

Bakshree Mishra, Dipam Chakraborty, Srajudheen Makkadayil, Saurabh Patil and Bhaskar Nallani (Intel Corporation)

Abstract: "Machine vision using CNN is a key application in Industrial automation environment, enabling real time as well as offline analytics. A lot of processing is required in real time, and in high speed environment variable latency of data transfer makes a cloud solution unreliable. There is a need for application specific hardware acceleration to process CNNs and traditional computer vision algorithms. Cost and time-to-market are critical factors in the fast moving Industrial automation segment which makes RTL based custom hardware accelerators infeasible. This work proposes a low-cost, scalable, compute-at-the-edge solution using FPGA and OpenCL. The paper proposes an methodology that can be used to accelerate traditional as well as machine learning based computer vision algorithms."

PAPER … **SLIDES**

Track 3.2: System Software and AI-2

Session Chair: Deep Varadarajan, Mediatek

Regular Paper: R**4**

An Optimal Resource Sharing Algorithm for Multi-Sim UE with Single RF Subsystem

Ruchi Kansara, Jitendra Otwani, Niladri Paria and Dr. Sajal Das (Intel Technologies)

Abstract: "With the evolution of wireless broadband technology and increasing demand of multi-sim User Equipment (UE), new challenges of resource sharing arise where conventional methods of creating small gaps in resource usage pattern of one SIM do not suffice. The advent of Voice over LTE (VoLTE) services accompanied by the immense mobile broadband demand of the users, require continuous resource availability on both the SIMs even in a single RF subsystem. Dual SIM Dual Active (DSDA) architecture that can meet the above requirements is not popular due to higher associated cost. In this paper, we consider the fundamental problem of resource sharing across SIMs in multi-sim architecture especially Single Receive Dual SIM Dual Standby (SR-DSDS) and Dual Receive Dual SIM Dual Standby (DR-DSDS). We formulate resource sharing as an optimization problem to maximize the ratio of resource allocation fairly for each contending SIM considering several important factors like current buffer occupancy, average time criticality of the buffer content and channel quality of respective SIM. We solve the formulated optimization problem using Karush Kuhn Tucker (KKT) conditions to derive the closed-form expressions for optimal resource allocation. We also compute the number of transitions possible with the derived optimal fair allocation in a practical multi-sim architecture. Additionally, we present the analytical results to depict the efficacy of the algorithm."

PAPER … **SLIDES**

Regular Paper: R**75** … Best Paper Winner (Software)

Enhancing eMMC with Multi-Stream

Sushma Vishwakarma, Anantha Sharma and Sharath Kodase (Samsung Semiconductor India R&D Center) Samsung Electronics Bangalore, India

Abstract: "Multi-stream for SSD is a concept where the host writes data with similar expected life times to contiguous blocks of NAND memory. Consequently this data has higher chances of being invalidated together. During garbage collection (GC), there will be minimal valid pages to copy, resulting in improved endurance and decreased write-amplification factor. Implementing Multi-stream in eMMC devices presents challenges due to lower DRAM, lower computational resource available. Maintenance of stream related information requires increase in DRAM usage, transfer buffer usage as well as addition computation for GC of stream related memory area. In this paper, we examine implementation of Multi-Stream concept in eMMC despite its low resource constraints. We have experimented with an implementation that supports up to 4 streams which uses additional ~108 bytes of DRAM and ~104 bytes of code section, and improves WAF by ~50% on FIO (File Input/Output) benchmarking setup where lifetimes are simulated by multiple instances of FIO."

PAPER … **SLIDES**

Regular Paper: R**121**

Storage Offload on SmartNICs

Purna Chandra Mandal, Nayana Mariyappa, Souryendu Das and Anbuvelu Venkataraman (Network Division Software Cloud Team, Data Center Group, Intel)

Abstract: "Cloud Service Providers (CSPs) nowadays are servicing huge amount of network and storage traffic in their data centers imposing huge cost and burden on their server system. The problem becomes worse with the introduction of virtualization technologies which increases traffic manifolds. Applications such as software-defined storage (SDS) and big data also increase traffic between servers, and often Remote Direct Memory Access (RDMA) is used to accelerate storage data transfers between servers. In this paper we propose to virtualize the storage capabilities of the host server and offload them to a SmartNIC, reducing load on host CPU, making the system robust in a cost effective way. We also demonstrate that SmartNICs can do this virtualized networked storage in a more efficient, easier to manage and look-a-like to local physical storage."

PAPER … **SLIDES**

Poster Papers

Poster Paper: P**51**

RapidNet IP protocol based Electronic Shelf Label (ESL) Solution

Kaveri Banakar and Shruthi Shetty (Analog Devices)

Abstract: "Electronic shelf labels (ESL) are electronic equivalent of price tags in retail stores, product id labels in large warehouses, and instruction sheets in manufacturing assembly lines. The volume of labels varies up to 1000-12000 in numbers depending on the application. This paper describes novel wireless protocol RapidNet IP and data compression algorithm used to update the ESL tags remotely. RapidNet IP is a secure & synchronized high throughput, low power & long-range wireless networking protocol. This is capable of updating 12000 ESL tags in one hour. Time Synchronized channel hopping (TSCH) method allows for congestion free traffic for larger number of nodes. The proprietary joining method allows the faster network formation. Data compression algorithm developed as a part this protocol compresses ESL tag PNG image from 150kb to 2kb. This facilitates the ability to update more tags in a short period and reduces the nodes wakeup time. This enables the low power wireless network end nodes battery life up to 7 years (with CR2450 x2 (2.9" ESL tag))."

PAPER … **SLIDES**

Poster Paper: P**82**

Integrated Cloud Cockpit: Making Surveillance and Maintenance of Oil Pipelines Practicable

Garima Srivastava, Yeshwant More and Jenifer Sam (SAP Labs India Pvt. Ltd.)

Abstract: Building a secure platform to connect distributed products, software and hardware simplifies digitalization of businesses. This calls for platforms that can help companies ideate, prototype, validate and develop using cutting edge technologies such as Artificial Intelligence, Internet of Things, Block Chain, Big Data and Analytics. In this paper, we illustrate how such Integrated Cloud Cockpits (ICC) provide a seamless environment with services that facilitate development of next generation smart applications that are scalable, resilient and provide decreased price-performance ratio. We support this research by presenting an empirical study on how intelligent surveillance and predictive maintenance of oil pipelines is made practicable by employing collaborative cloud services. We have leveraged the services provided by Google Cloud Platform to show how existing cloud platforms can suffice the needs of a secure and fully featured enterprise use case.

PAPER … **POSTER**

Poster Paper: P**84**

ART for Optimized Repeater Flop Network in Hard IP Design

Shweta Sharma, Rahul S Bhat and Shyam A (Intel Technologies, Bangalore, India)

Abstract: In all Hard IP (HIP) designs, there is a need for signals to travel from its source to destination module. To meet timing, they are flop repeated, based on the floorplan of the design. Different signals have unique repetition requirements based on their functionality/timing criticality. Also signals may have single destination or multiple destinations.
The flop repeater structure for each signal should be optimized so that it has minimum number of flops and timing is also met, to achieve desired targets for timing, area and power. This paper will show how we are create optimized tree structure based on mathematical techniques and generate automated RTL for such repeater flop module. This submission presents a new tool ART (Auto Repeater Tool) that completely eliminates the manual effort/time required to generate functional, ready to plug-in RTL.

PAPER … **SLIDES**

Poster Paper: P**86**

GROUND CHECKOUT SIMULATOR FOR TESTING CCSDS TELEMETRY & TELECOMMANDING

Parul , Soumya Subhra Banerjee, Mukul, Sangeetha K, Vithal Metri (Spacecraft Checkout Group, U.R. Rao Satellite Centre, Bengaluru, India)

Abstract: Ground checkout System is used for conducting the exhaustive tests at integrated spacecraft level to evaluate and qualify the functional performance of all subsystems onboard and ascertain the spacecraft is flight worthy. Telecommanding & Telemetry reception plays a vital role during integrated satellite testing and therefore a reliable Checkout System is required. To accurately predict and deliver high quality of service, checkout designers increasingly turn towards computer models of their systems to simulate real-time operating conditions and gain insights into usability and requirements prior to final product sign-off.
CCSDS format of telemetry and telecommanding is implemented in ISRO Satellites. CCSDS Telecommand and Telemetry Simulator is a software module developed to test and evaluate the functional performance of Telecommanding & Telemetry Acquisition in Checkout.

PAPER … **POSTER**

Poster Papers … Continued-2

Poster Paper: P**105**

Latch Based Designs: Advantages, Challenges and Solutions

Neelam Maniar, Vasudev Anand B, Shikha Subudhi, Hitesh Khandla and Gopalakrishnan Sadagopan (Intel Corporation)

Abstract: "Latches provide better alternative to flip flops in high frequency design's performance due to its inherent advantages of time-borrowing. Transparency of the latches creates timing paths through the latches as if the latches are repeaters. This comes with challenges of converging the designs with huge number of cycles' paths depending on number of transparent latches in the design. The paper presents a unique way of inferring the type of latch based designs and its generic bottlenecks. It also provides the way to generate the constraints to guide the Synthesis and Place & Route (PnR) Tool which helps improve the design quality that aids faster convergence of design parameters. It further talks about the sequential loops commonly encountered in pure latch based designs, its associated challenges and solutions for Synthesis and PnR designs."

PAPER … **POSTER**

Poster Paper: P**109**

'Welkin' – Parenting App and Analytics Engine using an IoT Framework

Swadha Pathak, Heenu Gupta and Tushar Vrind (Samsung Semiconductor India R&D Center) Samsung Electronics Bangalore, India

Abstract: "In today's world of rapidly growing connectivity technology, everyone is busy with their tech-gadgets on social and immersive media. Lives revolve around the internet and folks are busy catching up with and following the latest trends. Due to work commitments and hectic office schedules, adults lack in giving the required attention to their off-springs. This is deeply impacting the lives of kids. Kids suffering from different mental and physical disorders are left unnoticed at the initial stages causing serious issues at later stages that completely change their personality. Even for non- working parents, it is not possible to closely monitor kids during playtime or in school. Thus, several problems are left ignored. While there are available monitoring solutions, they are either too intrusive or leave the problem solution identification to the parents. There is a need to bring in available knowledge base to parents, to both understand the problem as well as to solve them. This paper proposes a novel solution - 'Welkin' as a kid-wearable and analytical engine, which captures and analyzes events & data, recognizes patterns learnt a priori from pediatrics and physiology, to create meaningful recommendations and follow-ups for parents. Recommendations enhance kid's capabilities by helping alleviate potential behavioral and situational risks, allowing the parent to focus their time and energy on the right thing – enjoying parenting!"

PAPER … **POSTER**

Poster Paper: P**135**

Power Conservation For VoNR Devices

Kashmira Kapoor, Prasad Dandra, Shrinath Ramamoorthy and Tushar Vrind (Samsung Semiconductor India R&D Center) Samsung Electronics Bangalore, India

Abstract: "With the introduction of 5G New Radio (NR), telecom operators are planning to integrate network elements of NR in different configurations for a phased and overlaid deployment and coexistence with 4G. Third Generation Partnership Project (3GPP) standardizes the deployment operation mode of the next-generation network, viz. working in Stand Alone (SA) NR scenarios and Non-Stand Alone (NSA) NR mode scenarios. Specifically as defined in the specification, Option 7 is where UE connects to 5G Core Network (5GCN) via either 4G enhanced Node B (eNB) cell or 5G next-generation NodeB (gNB) cell. Voice services available in 5GCN are referred to as Voice over NR (VoNR), and the power consumption for a User Equipment (UE) is dependent, on the physical resource allocation strategy in the serving cell. Available procedures of system selection defined in 3GPP are based on measurement of reference signal power levels, and priority criteria as defined in the System Information of the 5G/4G network. In this paper for the first time, we have discussed novel protocol and algorithm through which the UE maintains a history of availability of features like Semi-Persistent Scheduling (SPS), Connected Mode Discontinuous Reception (CDRX) and VoNR in the serving area of a cell, and uses this information later, during system reselection evaluation due to mobility. Through our proposed changes, a UE a) gets VoNR service more often and b) conserve more energy when the user activates VoNR service. We present an analytical model and through simulation show that during VoNR service, power is conserved due to SPS and CDRX on the selected cell."

PAPER … **POSTER**

Poster Papers … Continued-3

Poster Paper: P**143**
"MediaStratify" – Optimal paradigm in Multimedia Cloud Computing
Sreelakhsmi Gollapudi, Kartikeshwar Rath, Tushar Vrind, Deepak TY and Prasad R Rao (Samsung Semiconductor India R&D Center) Samsung Electronics Bangalore, India
Abstract: "In this era of digital communication, and explosion of social media, users generate and share a lot of information most of which is audiovisual content. This kind of multimedia content requires good amount of storage in the local device space as well at the network space. In the available parlance of multimedia cloud storage, when the content is streamed from the content server, the bit-stream is typically adapted depending on the available network bandwidth between the client and server session, for example by using Scalable Video Coding (SVC) technique. However, in case when the content is downloaded at the client for offline viewing, with say a resolution 'Low-Res-1', the multimedia clouds, do not offer additional mechanism to upgrade to a new resolution say 'High-Res-2', without downloading a new file version all over again. In this paper, we propose "MediaStratify" as a novel and optimal approach built on top of SVC to give a scalable solution for storing, sharing and upgrading the multimedia content for viewing offline. Based on the proposal, multimedia content will be stored as layers or 'stratified' and distributed over the cloud infrastructure. Through the devised protocol, the end node fetches the partial offsets (spatial, temporal or quality) and upgrades the files through reconstruction. Enterprise applications can utilize the scheme by installing the proposed novel combiner over the file transfer service, the solution can save network bandwidth and power consumption. The most important contribution is to bring down the Total Cost of Ownership (TCO) for any multimedia cloud or data center by reducing storage requirements by 50 ~ 74% over classical methods, yet achieve the goals of media hosting."

PAPER … **SLIDES**

Poster Paper: P**164**
Advanced Radio Link Manager to Support Mission Critical Services in 5G
Sree Lekshmi S and Seshaiah Ponnekanti (Amrita Center for Wireless Networks & Applications), Amrita Vishwa Vidyapeetham
Abstract: "Next generation networks or 5G will be "network of networks" that can support ultra-reliable and low latency communication, high data rate, huge connectivity and high security. Network transformation stirring towards virtualized Radio Access Network (v-RAN) and intelligent resource management are foreseen as key solutions to realise such varied 5G requirements. Effective Radio Resource Management (RRM) is crucial for Mission Critical (MC) services to underpin communication between smartphone, massive machines and tiny sensor devices. The paper explores pioneering research related to architecture and intelligent RRM that helps Service Providers (SPs) to design reference framework of an advanced Radio Link Manager (RLM) enabled by Machine Learning (ML). One example optimization for commercial network/Long Term Evolution (LTE) and some preliminary results are analysed to understand the reference framework. The paper addresses the general reference architecture framework of advanced Radio Link Manager to support Mission Critical services in 5G."

PAPER … **SLIDES**

Poster Paper: P**27**
DV Methodology to Model Scalable/Reusable Component to Handle IO Delays/Noise/Crosstalk in Mullane DDR PHY IF
Payal Joshi, Gaurav Kumar, Chethan Gowdra, Sriram Sounderrajan, Somasunder Sreenath and Tapas Jena (Samsung Semiconductors, India)

PAPER … **SLIDES**

Poster Paper: P**80**
An Automated and Scalable Fow for Mul-Paron RTL Generaon
Shru Narake, Karthikeya, Abhiram Peddiraju, Rajkumar Satkuri and Alok Anand (Intel)

PAPER … **SLIDES**

Poster Paper: P**130**
Methodology for Logic Opmizaon Post Synthesis
Sarala Gumma, Syed M Md Zaid Makandar and Neelam Maniar C (Intel)

PAPER … **SLIDES**

Poster Papers … Continued-4

Poster Paper: P**158**
Cheetah: Innovaon of Design System Infrastructure
Divya Ramarao, Mahesh Deshpande, Susmita Pal and Prateeksha Keshari (Intel)

PAPER … **SLIDES**

Poster Paper: P**112**
Mul-temporal End-to-end CNN: Audio-scene Classificaon, Speech Emoon
Pushpa Ramu, T, Vijaya Kumar, R Shunmuga Sundar, Anzar Zulfiqar, Rajeev Ranjan, Prashanth Narayan Jalli, Tilak Purohit and V Ramasubramanian (Samsung Semiconductors India)

PAPER … **SLIDES**

Demo

Demo: **21** … Best Demo Winner
Automotive Audio Bus®: Green Cars for a Greener Tomorrow
Suhasini Raghuram, Prasanna Thirumaleshwara and Karthik Radhakrishna (Analog Devices)

PAPER … **SLIDES**

Demo: **24**
Workforce Analycs with Career progression constraints (WAC)
Sampoorna Hegde (IBM)

PAPER … **SLIDES**

Demo: **30** … Best Demo Paper (Runner-up)
Real-time Audio Tuning Tool for In-cabin Applicaons
Krithika M S, Divya Venkatesh, John Joseph and Mohan Karthik P (Analog Devices)

PAPER … **SLIDES**

Demo: **38**
Automated QA for Cross Plaorm
Srima Sekaran, Anand Mutagond and Krishna Gopalakrishnan (Analog Devices)

PAPER … **SLIDES**

Demo: **52**
RapidNet IP protocol based Electronic Shelf Label (ESL) Applicaon
Kaveri Banakar and Shruthi Shey (Analog Devices)

PAPER … **SLIDES**

Demo: **85**
In field Tesng Soluon for Latent Fault Coverage
Sushma KA (Intel)

PAPER … **SLIDES**

Demo: **120**
An Introducon to Autonomous Driving and State Esmaon Using a Prototype
Saranya Das and Sriram Madavswamy (Analog Devices)

PAPER … **SLIDES**

Demo: **123**
Solar Tracking Using Thermoelectric Generator
Ananya S Bharadwaj, Prarthana Aithal, Sneha S, Divya B and Nagaraja Rao (Ramaiah University of Applied Sciences, Bangalore)

PAPER … **SLIDES**

Demo: **172**
Interoperable IoT Soluon for Smart Environments
Ritu Garg, Aiswarya Cyriac, Kalpana Mandapa (Intel)

PAPER … **SLIDES**

IEEE WINTECHCON-2019

Technical Conference by Women Engineers … 27 September 2019 … Bangalore

Hackathon

Hackathon WinTechCon 2019: Since Hackathons are a breeding ground for open innovation, fostering collaboration, learning new technologies and showcasing leadership in solving a technology problem, a Hackathon was arranged as a part of WINTECHCON-2019 for the women technologists and students. Totally 5 teams from Samsung, Intel and Texas Instruments India participated in the one-day event held prior to the conference on 20 September 2019. The teams showcased their work during the Hackathon track of the conference.

Team HW1: Smart Jewelry with theft or loss prevention Mechanism from Samsung

Rosarium Pila and Akash Kapashia (Samsung)

Team HW2: Search and Rescue through Slam from Intel India

Princess Samadharman, Ankit Dhingra, Ananya Goel, Anshuman Pattnaik, Mukesh Soni and Rajgopal Hariharan (Intel)

The other participating teams were:

Team HW3: Smart personal safety device

Veena Kamath, Vasudha Bhadoria and Himanshu Chaudhary (TI)

Team HW4: Roadway safety assistant

Pooja Madhusoodhanan, Yogeshwaran Shanmugam, Prashantkumar Sonavane and Karthik Rajakumar (TI)

Team HW5: Smart waste optimization and management system

Meghana Manavazhi and Shantanu Sampath (TI)

IEEE WinTechCon 2019 Hackathon Awards

- **Hackathon Winner (Hardware):**
  "Smart Jewelry with Theft or Loss Prevention Mechanism" – Rosarium Pila, Akash Kapashia, **Samsung**
- **Hackathon Runner-up (Hardware):**
  "Search and Rescue through Slam" – Princess Samadharmam, Ankit Dhingra, Ananya Goel, Ansuman Pattnaik, Mukesh Soni, Rajagopal Hariharan, **Intel**
- **Hackathon Winner (Software):**
  "Flythrough" – Priyanka Bose, Yasoda Aravapalli, BC Anuvarshini, H S Amrita, **Intel**
- **Hackathon Runner-up (Software):**
  "AI based Grammar Engine for SW Validation" – Yamuna Lingam, N Aparna, Om Aditya, Chandan Kumar, **Intel**