Latch Based Designs: Advantages, Challenges and Solutions

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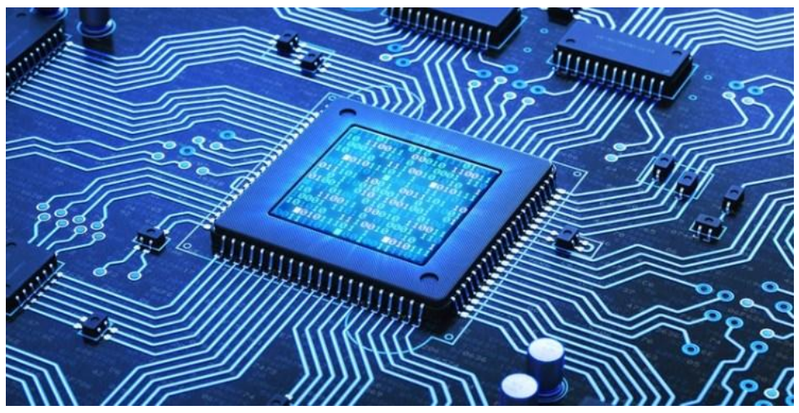
Latches over Flipflops:

- In flip-flop (FF) based designs, the longest pipeline between the two sequential elements limits the frequency of design.Latches provide better alternative to flip flops in high frequency design's performance due to its inherent advantage of unbalanced pipelines by time-borrowing.
- Transparency of the latches creates timing paths through the latches as if the latches were repeaters.
- In latch-based designs, if clock uncertainty after n-number of transparency cycles is x, in flip-flop based designs after n-stages, it will be nx. This helps boost the frequency of design further.

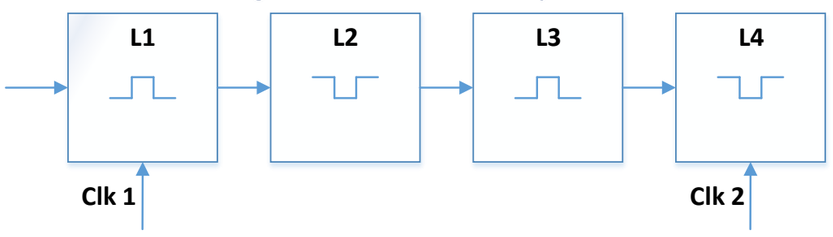


High speed design with Latches

Challenges

Transparency

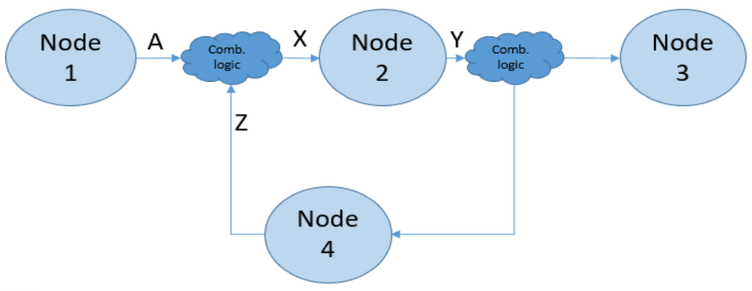
- Setup timing convergence of huge number of transparency cycle paths.
- Identification of appropriate constraints for the Synthesis and PnR Tool through bottleneck analysis.



2 Cycle Timing path from Clk1 -> Clk2 with L2 and L3 as transparent latches

Sequential Loops

- Sequential loop path is the one which starts from one sequential, passes through at least one transparent sequential and ends on the same sequential where it started.
- Loop setup margin is the difference in the arrival time at the endpoint of the loop before and after traversing the loop.

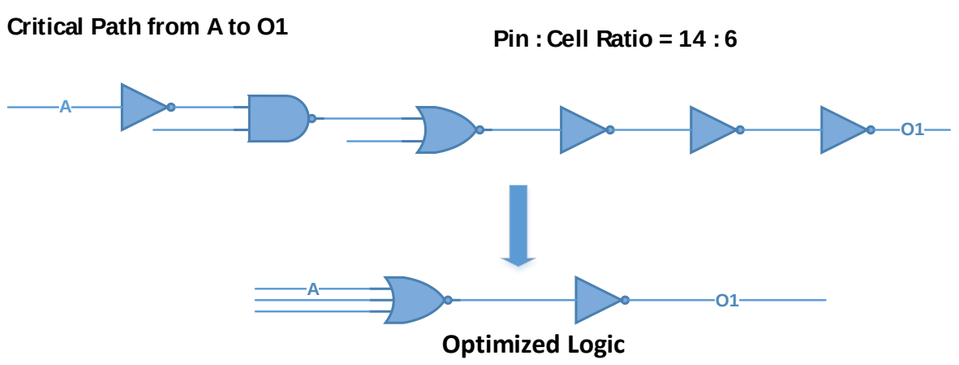


- Transparency on sequential loop latches causes infinite delay propagation if the loop setup margin is negative.
- The standard implementation tools, by default are designed such that the timing paths through transparent latches are considered as series of broken path segments between the latches.
- This results in un-converged loops in the design

Solutions

Transparency

- **Global Identification of long pole non-optimized logic:-** sequential pairs with number of combinational levels between the two, greater than the calculated optimal threshold are identified as bottlenecks.
- **Localized Identification of non-optimized logic and redundant repeaters**



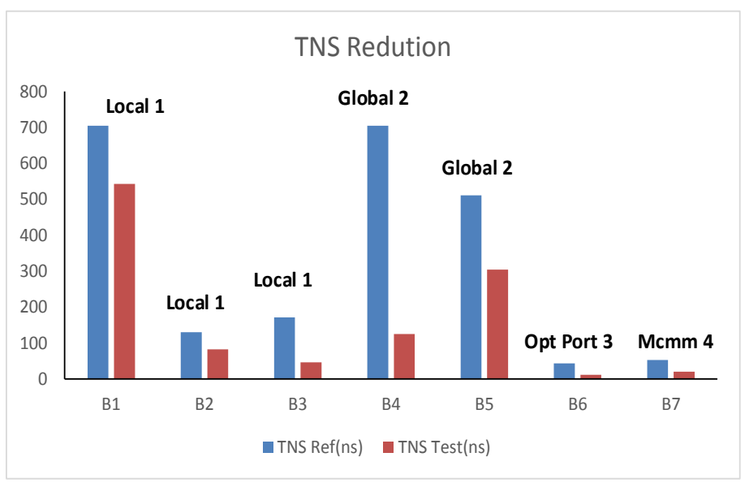
- **Optimal Cycle Time and MCMM constraints for synthesis:-** Just like flop based design, the average miscorrelation of delay between the EDA tools and signoff tool on critical paths is identified. The cycle time for synthesis is scaled accordingly
- **Identification of scenic placements:-** A ratio of total actual distance traversed by a critical path and the minimum possible traversal distance between the end points of the path (actual:minimum ratio) is calculated.

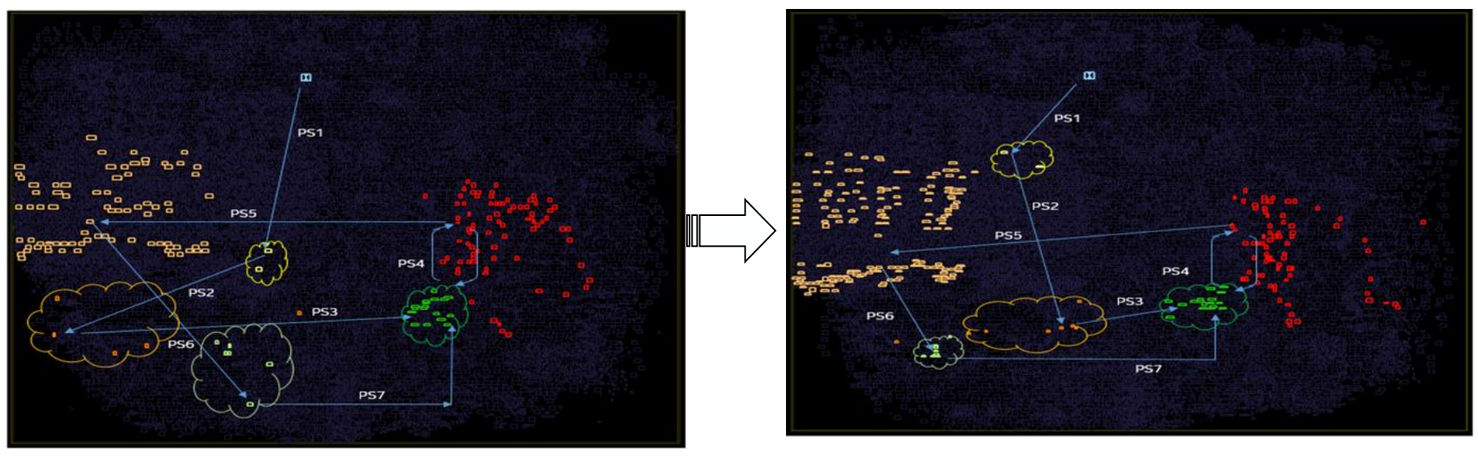
Sequential Loops

- Identifying the critical latches within sequential loops using bottleneck analysis
- Avoiding breaking of timing paths through these critical latches and allowing transparencies to be propagated for the EDA tools to optimize better.

Results

- Transparency:-The individual convergence utilities were piloted in Block designs B1, B2,…B7. This led to average 52% reduction of TNS, 5.24% reduction of dynamic power and 2.38% reduction of lkg power.
- Sequential loops: Identifying critical latches of the loop and avoiding breaking, led to 85% reduction in TNS and 8% reduction in lkg power





Seed Placement of critical latches of sequential loops improved, reducing the path length by 17.5%