WINTECHCON

Design and Verification Challenges with Third Party IP Cores

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Introduction

Context

- Priority of semiconductor design house ➔ Differentiating IP development in-house
- Mixed-signal SoC for portable, battery operated, autonomous embedded IoT market
- Low power and low cost are fundamental
- Focus on critical differentiators ➔ Analog, RF and power management (PM)
- Prefer third party IP cores ➔ Generic and foundational IPs
  Processors, embedded memories and mature standard driven connectivity functions
- Drivers: Time to market, better return on investment, increased focus and lower risk

Challenges

- Specification trade-offs or compromises
- Limitation with modification rights
- Limits flexibility and agility for evolving requirements
- Design, integration and verification challenges

Design Challenges & Proposed Solutions

Problem Statement

Challenges at IP design and SoC integration due to third party IPs

- Power, reset and clock (PRC) management scheme
  - Custom interface for PRC ⇔ IP, Assistant logic
- Mismatches in EDA vendor tools usage for SoC and third party qualification
  - Lint checks, waiver, outputs
  - Clock domain crossing (CDC) constraints, waiver, outputs
  - Reset domain crossing (RDC) constraints
- Inconsistency in memory mapped register definitions (due to scalability and configurability)
  - Assistant logic
- Mapping of standard protocol ⇔ Custom protocol usage in SoC
  - Protocol converter bridge development

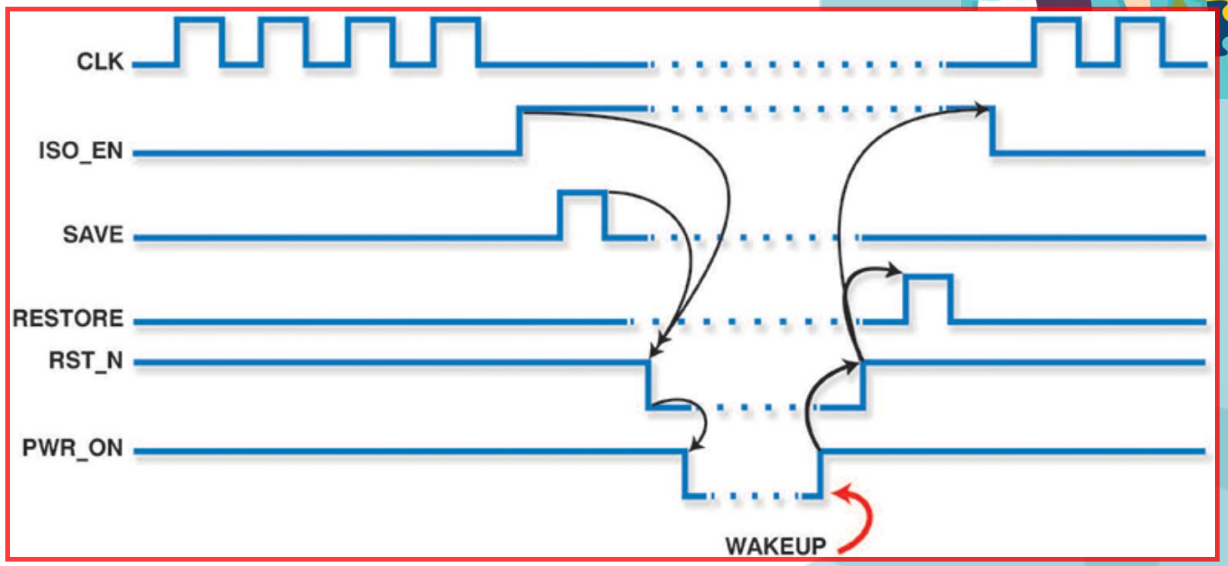
Power Sequence

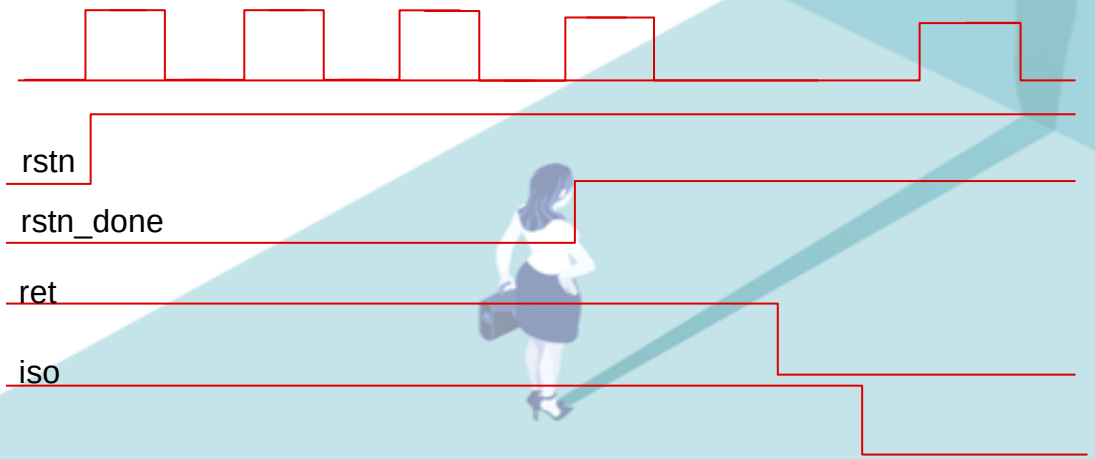
Problem

- Existence of reset synchronizers ➔ Failure of retention
- Clocks gated during entire power gating/un-gating sequence ➔ Failure of reset release

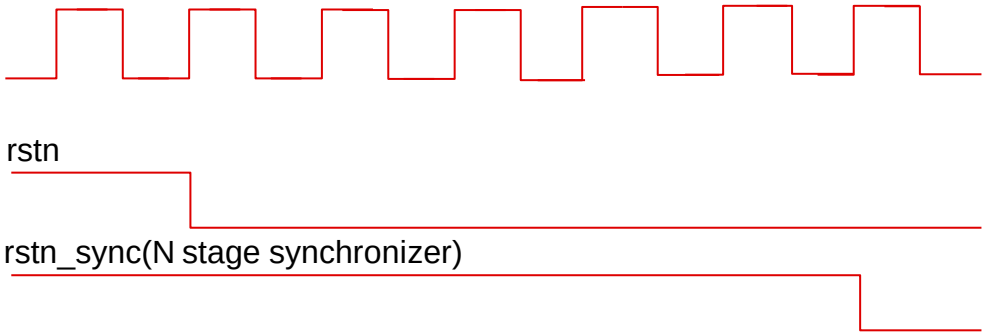
Solution

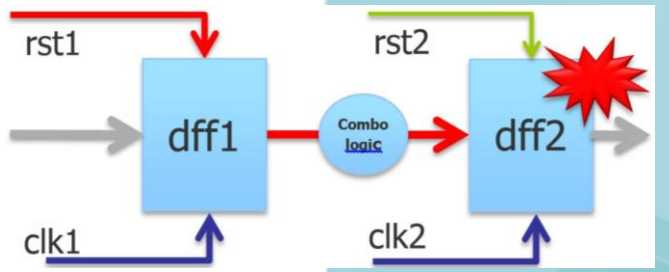
- Reset release acknowledgement to PRC controller
- Clocks availability during power un-gating sequence
- Clock free retention cell usage





Reset Sequence



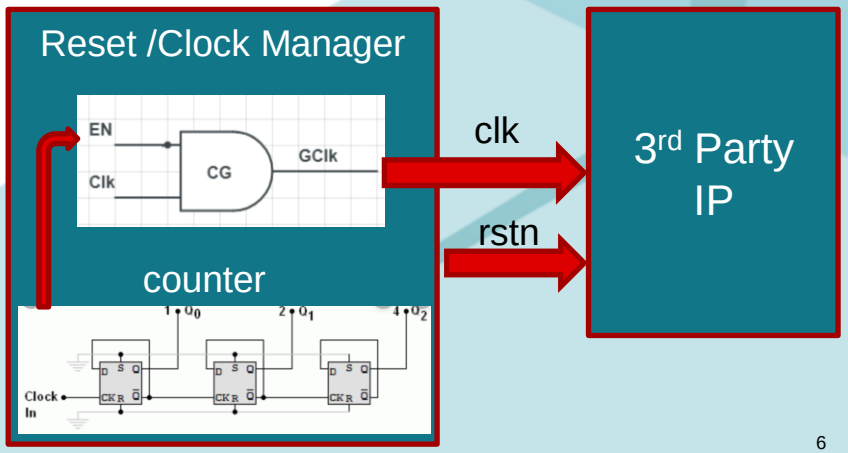


Problem

- Existence of synchronous reset
- Clock gating not achievable through reset isolation control
- Existence of RDC issues (IPs with multiple reset domains)

Solution

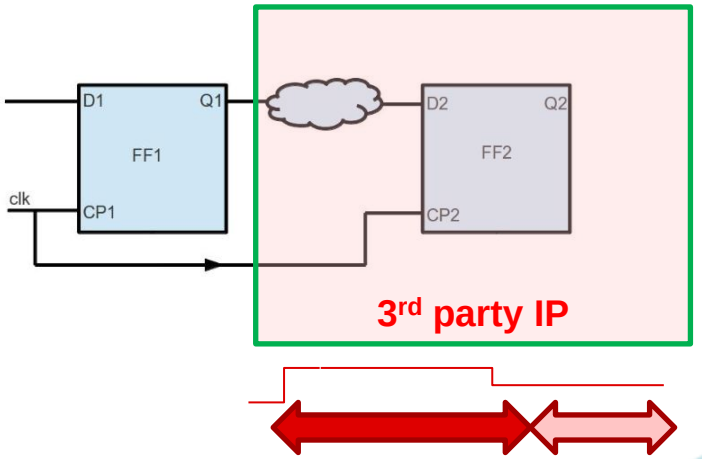
- Reset manager driven asynchronous reset duration
  - Counter to ensure N cycle reset assertion phase
- Custom clock gating for IP through PRC
- External clock gating using reset isolation



Timing Closure

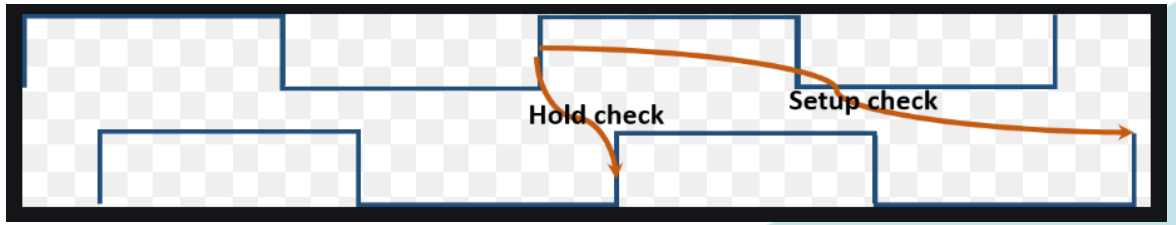
Problem

- High Input and High Output delays for CPU based 3rd Party IP
  - Area, Cost, Performance, Power



Solution

- Selective error correction in non timing critical paths and Re-fetch in critical paths. E.g. RAM vs Non volatile memory
- Stealing vs delaying
  - Clock skew vs Pipeline



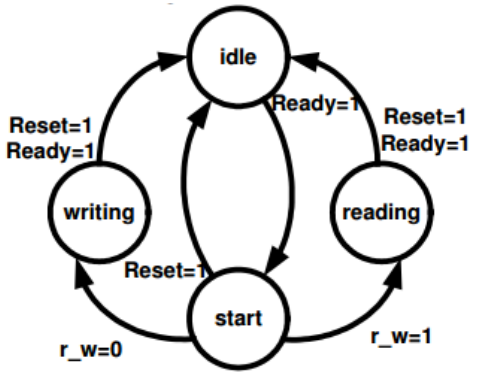
Memory Mapped Register (MMR) & Protocol Converter

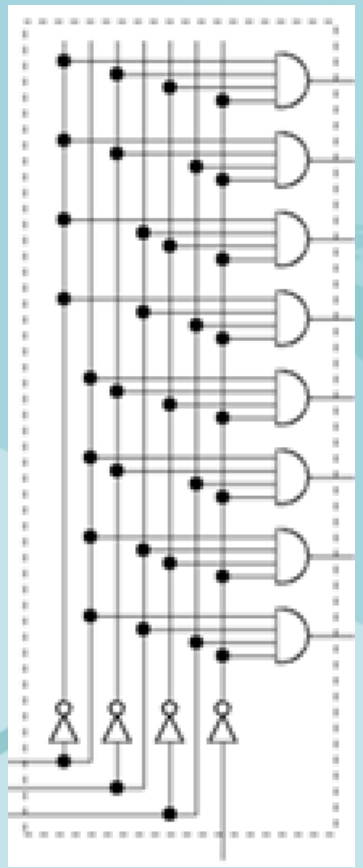
Problem

- Existence of non-applicable MMR's
- Standard protocol usage in 3rd party IP

Solution

- Redundant address decoder to ensure RAZ (Read as zero) and WI(Write ignore)
- Special software considerations ➔ "No support for certain MMR bit fields"
- Bridge development





Address Decoder

EDA Vendor Support

Problem

- Mismatches in LINT Checker Outputs per EDA vendor
  - Width mismatch between source (RHS) and target (LHS) arguments
  - Unused wire declarations
- Existence of Pseudo static CDC constraints (w/o detailed analysis)
- Existence of waivers to ignore convergence checks
  - Specifying points at or beyond ➔ no convergence of signals
  - Specifying net names ➔ Not checked for convergence

Impact:

- High Design bandwidth to review & disposition LINT/CDC warnings and Errors
- High DV bandwidth
  - Comprehensive verification and functional coverage for 3rd party IP

DV Challenges and Proposed Solutions

Problem Statement

Challenges in verification with third party IP integrated

- Power sequence verification
- Verification of parameterized third party IP
- RDC crossing inside third party IP
- Verification of system level bug fix
- Lack of IP ownership
- RTL and GLS mismatch
- Comprehensive verification of electrical specifications
- Mismatch in power intent format and low power verification

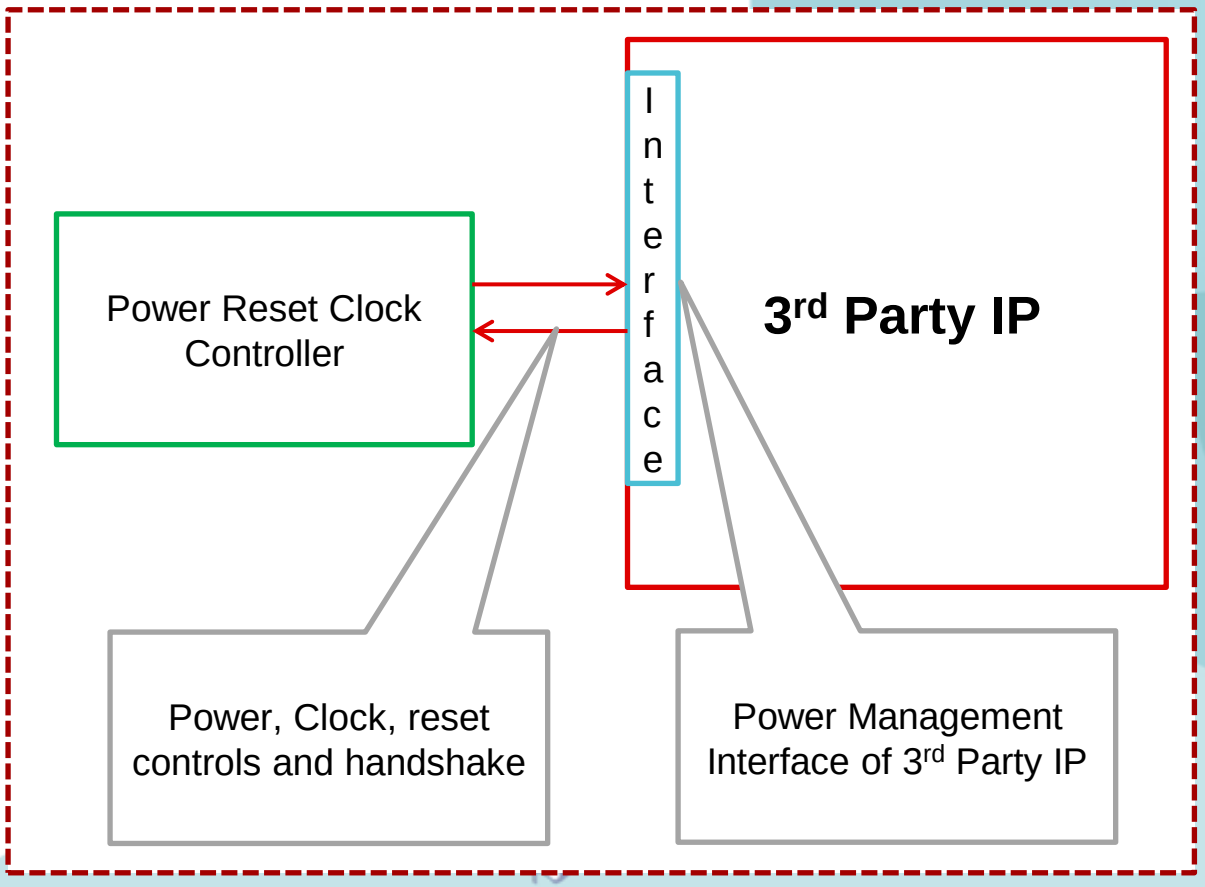
Power Sequence Verification

Problem

- Handshake sequence to ensure that reset synchronizers acquire proper values before retention is removed

Solution

- IP core abstracted to a fully randomized BFM with only power management interface



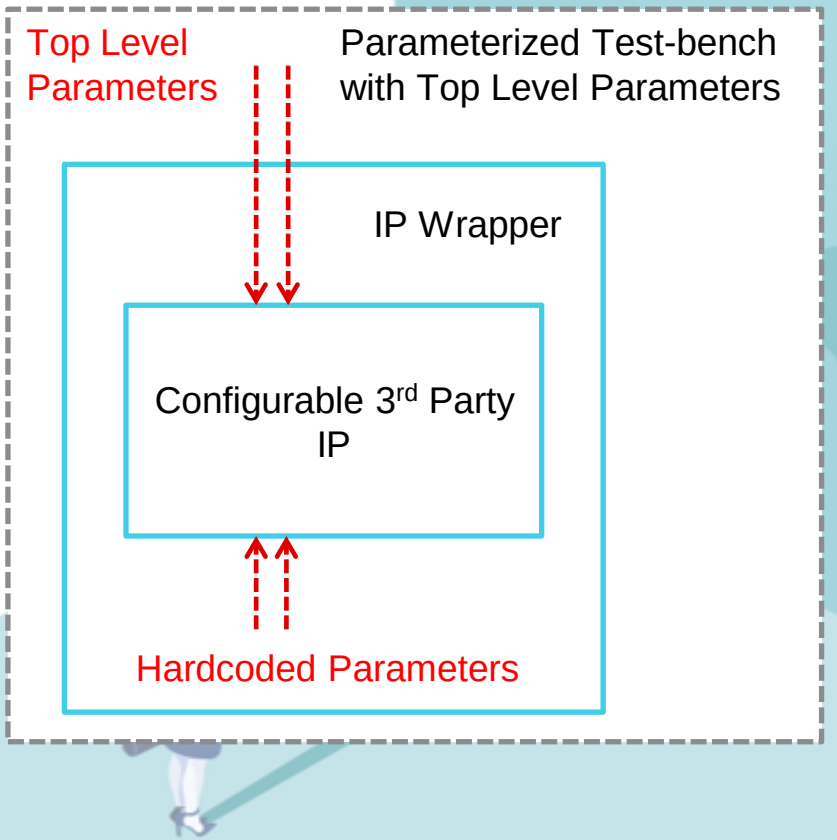
Verification of Parameterized Third Party IP

Problem

- Configurable parameters in 3rd party IP to optimize internal module functionalities
- Top level v/s hardcoded inside the wrapper

Solution

- Change of parameters: Registers inside 3rd party IP, functionality change
- Checks for maximum, minimum and typical values at SoC



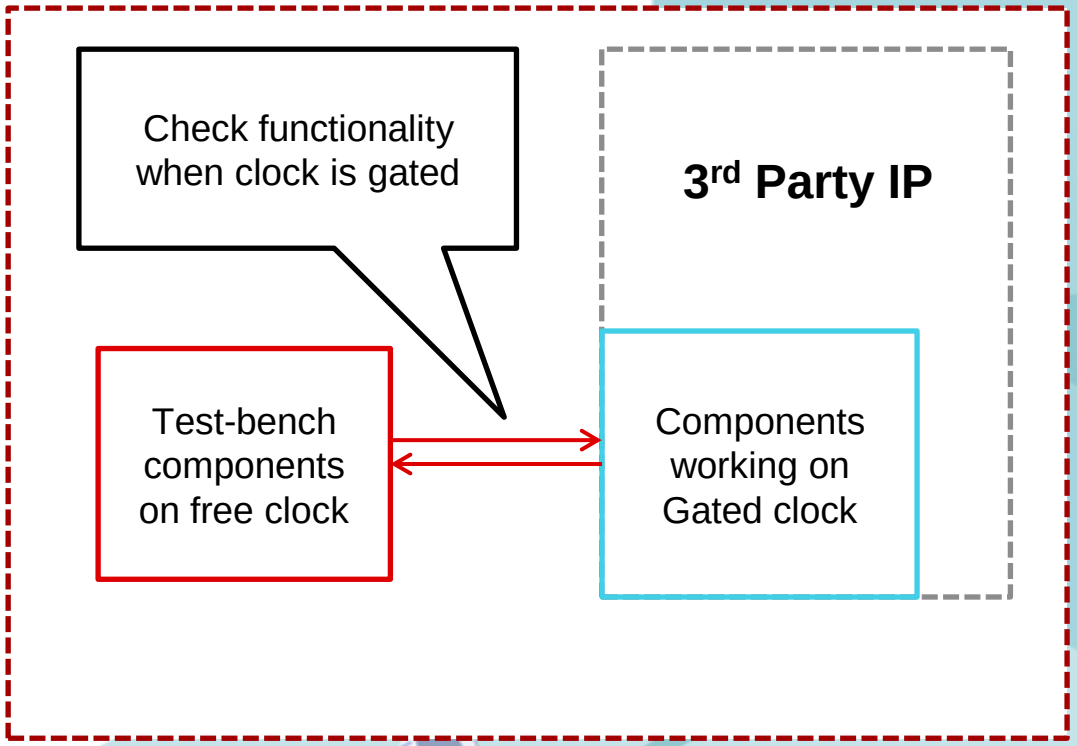
RDC crossing inside third party IP

Problem

- Thorough verification of Clock gating scheme associated with RDC crossing involving multiple power domains

Solution

- Add dedicated always running checks on the gated clock
- Example: Verification of debug path to third party core with RDC crossing



Summary | Design

S. No.	Challenge	Recommendation
A	Power	Custom interface with PRC, conditional clock un-gating
B	Reset	
C	Timing closure	Selective error correction & Time stealing vs Delaying
D	MMR	Redundant address decoders and software care-abouts
E	EDA support	Careful analysis and custom mapping of waivers, errors, etc.
F	Protocol bridge	Protocol bridges

Summary | Verification

S. No.	Challenge	Recommendation
A	Power sequence	Custom IP BFM for CRV of PM scenarios
B	Parameter	Custom parameterised TB
C	RDC fix validation	Clock gating checks for higher order resets when lower order resets are active
D	Convergence	Detailed coverage analysis with meta-stability injection
E	System design fix validation	Thorough IP verification with integration logic, if any, including with vendor verification vectors
F	IP ownership	Proactive knowledge base and training
G	RTL Vs GLS mismatch	Comprehensive GLS coverage with identified minimum set of critical scenarios
H	Electrical specifications	Detailed mixed-signal IP specifications, integration specification and verification plan
I	Power intent & low power	A well thought out LP integration and verification methodology

Conclusions

- Increasing size and complexity of modern silicon systems
- Drive for reusable, pre-verified third party IPs
  - Embedded memories, processors and high-speed interfaces
- Associated design and verification challenges
- This paper discussed
  - Some of the challenges
  - Best design practices and methodologies to overcome
- Applied in mixed-signal, low power SoC designs
  - Successful integration
  - Accelerated path to first pass silicon success

References

- "System Drivers: Mixed-signal Evolution," ITRS, 2011.
- Lakshmanan Balasubramanian, Puneet Sabbarwal, Rajesh Kumar Mittal, Prakash Narayanan, Ranjit Kumar Dash, Anand Devendrá Kudari, Srikanth Manian, Sudhir Polarouthu, Harikrishna Parthasarathy, Ravi C Vijayaraghavan, Sachin Turkewadikar, “Circuit and DFT techniques for robust and low cost qualification of a mixed signal SoC with integrated power management system,” Design Automation & Test in Europe Conference & Exhibition (DATE) 2011, pp. 1-4, 2011.
- Rajesh Mittal, Lakshmanan Balasubramanian, Adesh Sontakke, Harikrishna Parthasarthy, Prakash Narayanan, Puneet Sabbarwal, Rubin A. Parekhji, “DFT for Extremely Low Cost Test of Mixed Signal SOCs with Integrated RF and Power Management,” 2011 IEEE International Test Conference, pp 1-10, 2011.
- Rubin A Parekhji, Michael Nicolaidis, “SOC Design Readiness for Automotive Applications,“ Design Automation & Test in Europe Conference & Exhibition (DATE) 2013, pp. 1-4, 2013.
- Ashwini Kumary Padoor, Lakshmanan Balasubramanian, Ibukun O Olumuyiwa, “Unified Verification Methodology for Digital and Analog Mixed-Signal Co-Simulation for Low Power Embedded SoC,” IEEE WINTECHCON, 2018.
- Lakshmanan Balasubramanian, Venkatraman Ramakrishnan, Zhong Fan, Vijay Kumar Sankaran, Aswani Kumar Golla, Arumugan A, Rewin Edwin, Manash Ranjan Raiguru, Tutorial on “Modern Recipes for Brewing the Inevitable Methodology for Today’s ICs: Low Power Mixed-Signal Design Verification,” Design Automation Conference, 2019.

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Q&A

Thanks your for your interest, time and attention!