Optimized Battery Life For Ultra-Low Power Products

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Introduction

Battery life management for Ultra-Low Power products [Mobiles, Tablets, Notebooks, and Convertibles] is crucial in today's compute world

Constraint

Constraint

Thermal dissipation

Limits computational performance

Battery life management for ULP products

- Battery usage time is determined by power consumption of the device
- Battery life suite is introduced with real time use cases (KPIs) to analyse battery life of product and target to achieve x hours of battery life

Key Power Indicators (KPIs)
Web Browsing
Productivity
Music Streaming
Photo Capture
Idle Screen On
Video Conferencing
Video Streaming
Video Playback

$$Battery\ Life\ (Hrs) = \frac{Battery\ Size\ (W.Hr)}{Platform\ Power\ Consumption\ (W)}$$

Battery Life Optimization Features

The urge for devices with longer battery life in today's compute world has motivated multiple changes in the design, architecture, and SW optimizations.

Features focused here are

- Architecture/IP Features
- Software Features

Architecture/IP Features

These features are proposed based on the power savings they provide as well the need to provide a cost effective product with all the power and performance requirements being met.

1. Command mode panel :

a. panel has a buffer which can refresh the panel itself without asking any data from the memory if there is no change in the frame

b. Allows significantly lower active residency and DDR BW in the SoC

2. Clocking Optimization :

a. Redesigning clocking subsystem in the IPs with selective usage of high power PLLs and low power PLLs.

b. Opportunistically gating the clock distribution within the subsystem

Architecture/IP Features

3. Lowering of IO voltage

a. Enabling voltage binning capability on IO rail. (allowing faster parts to operate at lower voltage)

4. **LPDDR5 memory**

a. LPDDR5 introduces a deep sleep mode, which reduces the IDD current by 40% that in turn saves power.

Software Features

1. **PSR2 [Panel Self Refresh 2] :**
    a. PSR2 is the second level of Panel Self Refresh which allows memory to go into self refresh faster with reduced BW
    b. Selective fetch of the pixels from memory that change their values in a subsequent frame with respect to the current frame (dirty pixels) instead of entire frame.

2. **eDP mode power savings:**
    a. Transitioning from MIPI PHY to MIPI-eDP combo PHY.
    b. eDP mode supports increased drive impedance to reduce the drive strength
    c. eDP has HBR (5.4 Gbps per lane) in comparison to MIPI (1.5 Gbps per lane)

3. **Frequency vs. Residency tuning**:
    a. Operating CPU cores at power efficient frequencies.

Results

Power savings from architecture/IP features

Web Browsing Use case		
Feature	Details	Savings (%)
Command Mode Display Panel	Panel Self Refresh as it has internal buffer	10.2%
Clocking Optimization	Low Jitter/ LP PLL	1.3%
Memory Type	LPDDR5 used instead of LPDDR4x	3.7%
IO voltage lowering	To reduce the IO rail voltage	2.1%

BL Use cases	Command Mode	Clocking optimizations	LP5	lowering IO voltage	Total
Web Browsing	10.2%	1.3%	3.7%	2.1%	16.2%
Productivity	14.0%	1.2%	2.9%	1.6%	19.4%
Music Streaming	0.0%	1.0%	0.0%	1.0%	-1.9%
Photo Capture	0.0%	1.0%	5.3%	2.8%	8.0%
Idle Screen On	67.2%	0.0%	0.7%	0.0%	66.2%
Video Conferencing	0.0%	1.2%	5.7%	3.3%	8.9%
Video Streaming	15.9%	1.4%	3.7%	2.3%	21.9%
Video Playback 30 FPS	15.6%	1.3%	3.1%	2.0%	21.3%

Results

Power savings from Software features

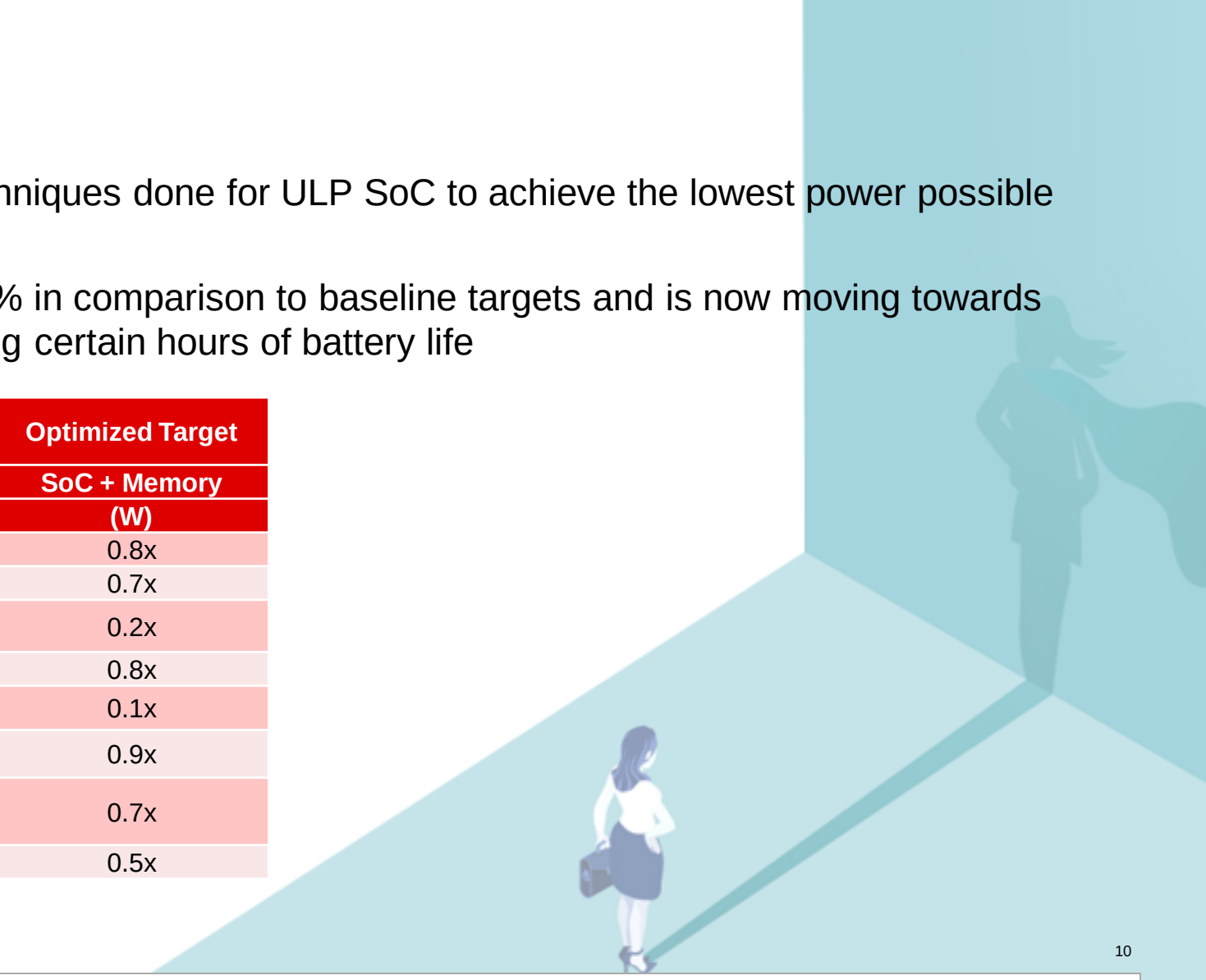
Web Browsing Use case		
Feature	Details	Power Savings
PSR2	Only dirty rectangles were read	18.9%
HBR2 Implementation	Impedance matching to reduce power	2.4%
Frequency vs Residency Tuning	Fix power optimized frequencies to be used	6.8%

BL Use cases	PSR2	eDP Mode	Total Savings
Web Browsing	18.9%	2.4%	21.7%
Productivity	19.4%	1.0%	20.9%
Music Streaming	0.0%	0.0%	1.0%
Photo Capture	0.0%	0.5%	1.0%
Idle Screen On	3.4%	0.0%	3.4%
Video Conferencing	0.0%	1.4%	1.4%
Video Streaming	4.1%	0.7%	5.0%
Video Playback 30 FPS	5.4%	0.9%	6.3%

Conclusions

- We discussed the optimization techniques done for ULP SoC to achieve the lowest power possible with the minimum set of changes.
- Overall BL has improved by ~11.5% in comparison to baseline targets and is now moving towards meeting the desired target of having certain hours of battery life

BL Use cases	Baseline Target	Optimized Target
	SOC+Memory	SoC + Memory
	(W)	(W)
Web Browsing	1x	0.8x
Productivity	1x	0.7x
Music Streaming	1x	0.2x
Photo Capture	1x	0.8x
Idle Screen On	1x	0.1x
Video Conferencing	1x	0.9x
Video Streaming	1x	0.7x
Video Playback	1x	0.5x



References

[1]Shivajit Mohapatra, Radu Cornea, Hyunok Oh, Kyoungwoo Lee, Minyoung Kim, Nikil Dutt, Rajesh Gupta, Alex Nicolau, Sandeep Shukla, Nalini Venkatasubramanian, "A Cross-Layer Approach for Power-Performance Optimization in Distributed Mobile Systems"

[2] Internal Publications